ZES
Zero-Error Systems Pte Ltd

Latchup Detection and Protection (LDAP)

Enabling Advanced Commercial-Off-The-Shelf (COTS) to 'Space-Grade'

LDAP

ZES' LDAP is a radiation-hardened monolithic chip that serves to detect and protect Commercial-Off-The-Shelf (COTS) from Single-Event Latchup (SEL). The single chip operates over an input range of 1.2V to 5V with the loading current range of 1mA to 0.5A.

ZES' LDAP is based on a proprietary technology (patent pending) offers an unprecedented means to protect COTS – enabling advanced COTS ICs to space. Specifically, LDAP incorporates two levels of protections. First, LDAP can detects the onset of the SEL occurrence. In other words, the response of LDAP to SEL is very fast, and LDAP can detect micro-SEL. Second, LDAP also provides an overall threshold for SEL current. Both cases can trigger power cycling of COTS.

LDAP is immune to Single-Event Transient (SET) and Single-Event Upset (SEU), and is unaffected by long-term drift current due to Total Ionized Dose (TID).

High integration makes LDAP an ideal candidate to accompany a COTS IC when being employed in space.

Features

- ❑ 10^2 – 10^6 higher protection over present practice
- ❑ <1μs response time to SEL
- ❑ Detection of the SEL occurrence in early stage
- ❑ Detection of micro-SEL (calibration is required)
- ❑ Protection of COTS ICs from destructive damage by power cycling
- ❑ Immune from current drift due to aging and TID
- ❑ Wide input voltage range and wide loading current range
- ❑ Ceramic QFN32L

Modalities

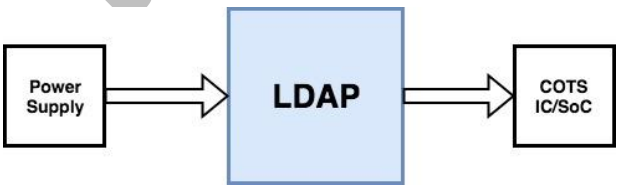
- ❑ Stand-alone
  - ❖ Protect COTS on PCB
- ❑ Integrated with COTS ICs/SoCs in System-in-Package
  - ❖ Bare die
- ❑ Monolithically integrated with COTS ICs/SoCs
  - ❖ IP core

Electrical Performance

Input Voltage	1.2V-5V
Nominal Loading Current	1mA-500mA
Response Time	<1μs
Power Cycling Time	<10ms (Adjustable)
Operating temperature	-55°C to 125°C

Radiation Performance

TID	500 Krad (Si)
SEL	50 MeV-cm^2/mg
SEFI	50 MeV-cm^2/mg
SEU	50 MeV-cm^2/mg
Ion Fluence	Up to 10^6/cm^2

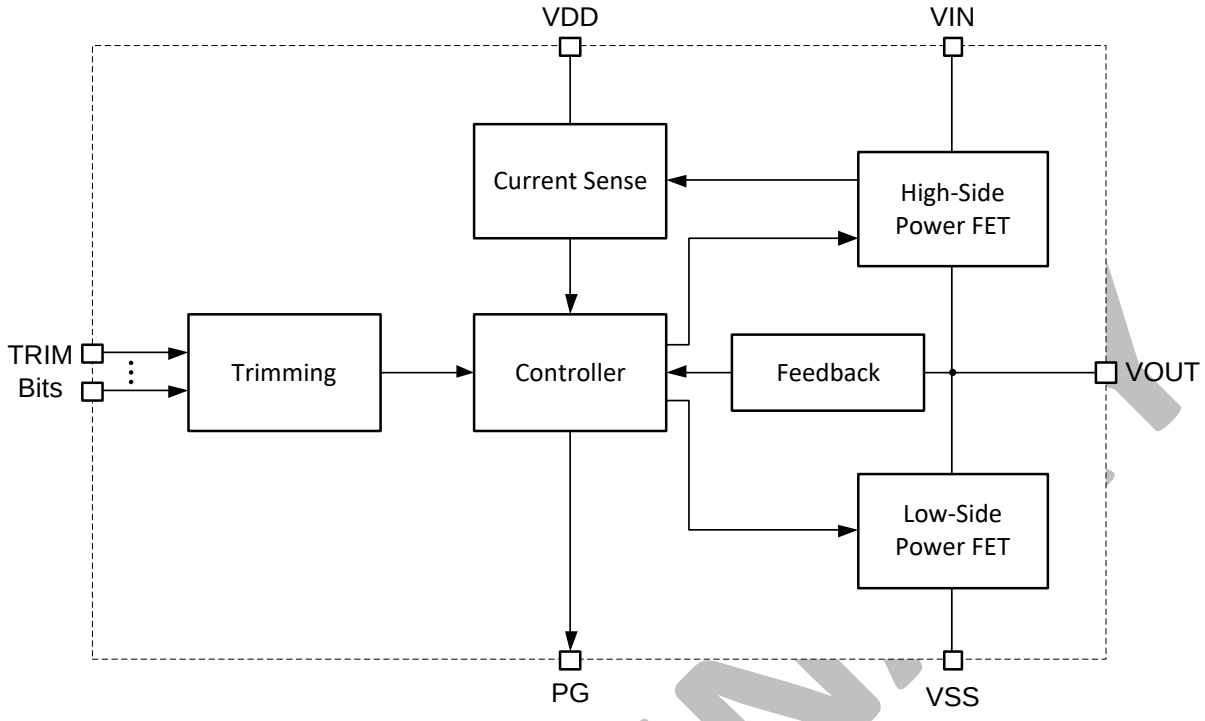


ZES (Zero-Error Systems)
Wei Shu, CTO
weishu@zero-errorsystems.com

05-07 TCH TechCentre
71 Toh Guan Road East
Singapore 608598

US Patent No.: 10,566,780 B2

Functional Block Diagram



Ordering Information

Part Number	Temperature Range (ºC)	Package
LDAPxxx	-55 to +125	32L Ceramic QFN

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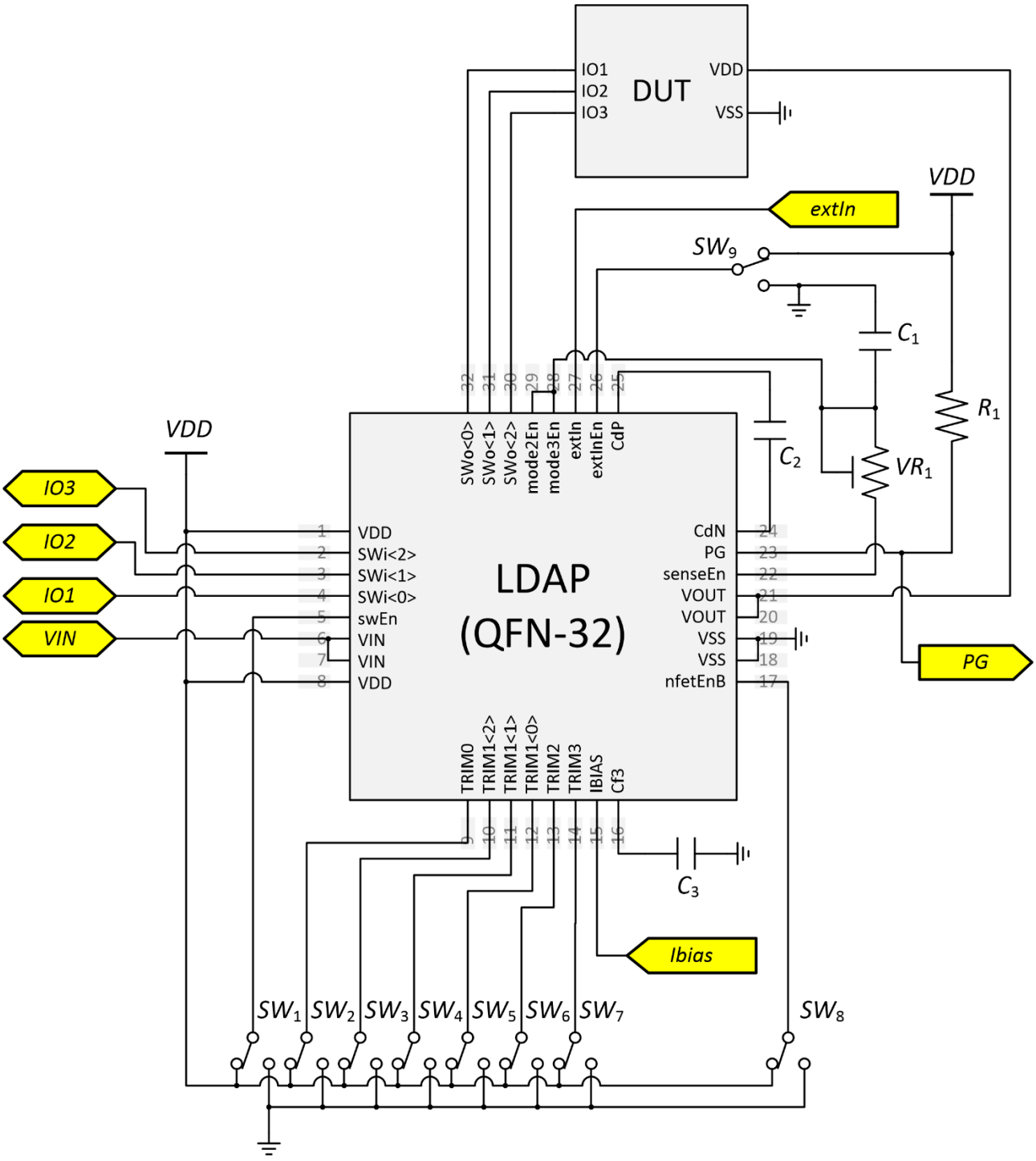

Figure 1 Schematic of the test bench of the LDAP and DUT

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Pins for LDAP

Pin No	Name	Type/Description
1, 8	VDD	Bias supply to the LDAP circuitry.
2-4	*SWi<2:0>*	IOs of the internal switches.
5	*swEn*	Input that enables internal switches.
6-7	*VIN*	Power supply input.
9	*Trim*0	Input trimming bit to calibrate *VOUT* drop-out voltage.
10-12	*Trim*1<2:0>	Input trimming bit to calibrate Mode 1 detection.
13	*Trim*2	Input trimming bit to calibrate Mode 2 detection.
14	*Trim*3	Input trimming bit to calibrate Mode 3 detection.
15	*IBIAS*	Bias current input.
16	*Cf3*	Connect this pin to the feedback capacitor.
17	*nfetEnB*	Active low input that enables low-side power FET.
18-19, Ground plane	*VSS*	Ground.
20-21	*VOUT*	Output of the power block.
22	*senseEn*	Output that provides sensing enable signal.
23	*PG*	Power-Good output. Open-drain logic output that indicates *VOUT* status.
24	*CdN*	Connect this pin to the delay capacitor.
25	*CdP*	Connect this pin to the delay capacitor.
26	*extInEn*	Input that enables *extIn*.
27	*extIn*	Input that bypasses the control of the power transistors.
28	*mode3En*	Input that enables Mode 3 detection.
29	*mode2En*	Input that enables Mode 2 detection.
30-32	*SWo*<2:0>	IOs of the internal switches.

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