ZSOM-F01
FPGA-ZU3EG Based System-on-Module

V1.1a Apr 2026

Radiation-Tolerant System-on-Module with FPGA

AMD Zynq™ UltraScale+™ MPSoC ZU3EG C784

Enabling Advanced Commercial-Off-The-Shelf (COTS) to 'Space-Grade'

Product Overview

ZSOM™ is a family of ZES' Radiation Tolerant System-on-Modules (SoMs) for processing platforms that leverage on Power-reliability and Data-integrity solutions to protect commercial-off-the-shelf (COTS) components from radiation effects.

ZSOM™-F01 is a Rad. Tol. SoM embodying **FPGA AMD Zynq™ UltraScale+™ MPSoC ZU3EG C784** with **Single-Event-Latchup (SEL) and Single-Event-Upset (SEU)** mitigations. ZSOM™-F01 enables a quick and reliable payload development platform for data-intensive high-performance computing Space applications.

Key Features

- FPGA-based SoM is integrated with SEL and SEU protections:
  - SEL protection enabled by ZES100 Radiation-Hardened Latchup Detection and Protection (LDAP-IC) x 3pcs.
  - SEU protection enabled by Triple-Modular-Redundancy (TMR) ZES400 Radiation-Hardened Voter-IC with external FRAMs (3pcs) and proprietary Error-Detection-And-Correction (EDAC) C-code for detecting/ correcting multi-bit soft errors, suitable for BRAMs (within FPGA), Flash, eMMC, and DDR memories.
  - 2,000x less soft-errors than Single-Error-Correction-Double-Error-Detection (SECDED).
- High Reliability Manufacturing PCB
- Operating temperature (TVAC): -30°C to 60°C
- Power Input: 12V@2A (max.)
- Small Formfactor (90.17mm x 81.70mm)

ZSOM™-F01 Specifications

- **AMD Zynq™ UltraScale+™ MPSoC device XCZU3EG-1SFVC784I**
  - Arm Quad-core Cortex™-A53 1.2GHz
  - Arm Dual-core Cortex™-R5 500MHz
  - Mali™-400MP2 GPU 667MHz
- DDR4 SDRAM (4GB for PS, 1GB for PL)
- QSPI Flash (256Mbit)
- eMMC Flash (32GB)
- 180 user PL I/O pins and 26 user PS MIO pins (one full MIO bank) via 4 connectors
- Supports 10/100/1000Mbps Gigabit Ethernet (1x PS, 1x PL)
- Supports SATA3.1, USB2.0, USB3.0, PCIe2.0/1.0 x4, and Display Port (Shared GTx)

Target Applications

- Payload designs for Space missions for VLEO, LEO, MEO, GEO with radiation protection against SEL/SEU
- Earth Observation (EO) payloads
- Telemetry, scientific data processing payloads (Image-sensing, AI and/or edge-computing)
- Navigation, instrumentation payloads (e.g., star trackers, gyroscopes, accelerometers, etc.)
- Application-specific software-enabled payloads (e.g. security codes/protocols, etc.)
- Low error-rate data protection applications

ZSOM-F01: Rad. Tol. System-on-Module

ZSOM-F01-T01: Carrier board Evaluation Kit (EVK) for ZSOM-F01

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1 Overview

ZSOM™-F01 is a high-performance FPGA system-on-module (SoM) based on AMD's Xilinx's Zynq UltraScale+ MPSoC (device XCZU3EG-1SFVC784I). It integrates a powerful Processing System (PS) featuring quad-core ARM Cortex-A53 processors (up to 1.2 GHz) and dual-core Cortex-R5 processors (up to 500 MHz) along with a robust Programmable Logic (PL) section. The SoM is designed for demanding applications in space and high-reliability environments. It features five DDR4 DRAM chips (four on the PS side forming a 64-bit interface with a total capacity of 4GB, and one on the PL side providing a 16-bit interface with 1GB), a 32GB eMMC flash for boot storage, system files and user data, and a 256 Mbit QSPI flash for boot storage (if necessary). The design adheres to CubeSat/PC104 specifications for space applications and includes integrated radiation protection circuits such as ZES100 LDAP (micro-SEL/SEL detection) and ZES400 VOTER with 1 Mbit FRAM Triple Modular Redundancy (TMR) SPI function and ZES' EDAC algorithm (bit-flips, soft-errors detection and correction).

1.1 Ordering Information

Part Number	Description	Size
ZSOM-F01	ZSOM-F01 FPGA-ZU3EG Based System-on-Module	**90.17mm x 81.70mm**
ZSOM-F01-T01*	ZSOM-F01-T01 Evaluation Carrier board for ZSOM-F01	**180mm x 120mm**

*ZSOM-F01-T01 is the corresponding carrier board Evaluation Kit (EVK) for ZSOM™-F01. The ZSOM-F01-T01 is designed and tested only for ground conditions and at room temperature.

For further price, delivery, and ordering information, please contact sales@zero-errorsystems.com

2 Features

- **High-Performance Processing:**
  - AMD's Zynq UltraScale+ MPSoC (XCZU3EG-1SFVC784I) featuring quad-core Cortex-A53 (up to 1.2 GHz) and dual-core Cortex-R5 (up to 500 MHz).
- **Memory Configuration:**
  - DDR4 DRAM (MT40A512M16LY-062E): Four chips on the PS side provide a 64-bit data bus and a total capacity of 4GB; one chip on the PL side offers a 16-bit data bus with 1GB capacity.
  - QSPI Flash: 256 Mbit (MT25QU256ABA1EW9) for boot image storage.
  - eMMC Flash: 32GB (MTFC32GAPALBH-IT) for system and user data storage.
  - FRAM: 3pcs of 1 Mbit (MB85RS1MTPW) implemented in TMR.
- **High-Speed Interfaces:**
  - Multiple high-speed I/O ports including PCIe 2.0, PCIe 1.0, SATA3.1, USB2.0, USB3.0, Gigabit Ethernet (10/100/1000Mbps), and extensive Multiplex IO connectivity.
  - Other supported interfaces: UART, CAN, SPI, I^2C.
  - Four 120-pin board-to-board connectors for direct interfacing with base/carrier boards.
- **Clock and Power Management:**
  - PS system clock provided by a 33.333 MHz crystal and a differential 200 MHz PL clock source for high-speed DDR4 interfacing.
  - Power supplied via a +12V input managed by the PMIC TPS6508641.
- **Robust Design for Space Applications:**
  - Conformant with CubeSat/PC104 standards.
  - Integrated protection circuits include ZES100 LDAP-IC for Single-Event-Latchup (SEL) detection/protection x 3pcs.
  - Integrated ZES400 VOTER-IC for TMR FRAMs for soft-error/Single-Event-Upset (SEU) mitigation.
  - Proprietary Error-Detection-and-Correction (EDAC) algorithms for protecting DDR4, QSPI Flash, eMMC Flash, and embedded BRAMs in FPGA.
  - e-Fuse (TPS259813APRWR) for over-current/voltage protection on the +12V power line.

3 Block Diagram

Figure 1 depicts the overall architecture of the ZSOM™-F01 module, centred around the AMD Zynq UltraScale+ MPSoC ZU3EG. On the memory side, the module integrates four DDR4 chips (64-bit interface) and one DDR4 chip (16-bit interface), as well as QSPI Flash and eMMC Flash for firmware and operating system storage. Additionally, FRAM is configured with Triple Modular Redundancy (TMR) and protected by the ZES400 Voter to mitigate soft errors (SEUs). The ZES100 LDAP chip monitors SEL events and safeguards the power supply in coordination with the e-Fuse and onboard voltage regulators. Finally, four board-to-board connectors (J29, J30, J31, and J32) provide high-speed interfaces and expanded I/O for the module, completing a robust system-on-module solution suitable for demanding embedded and space applications.

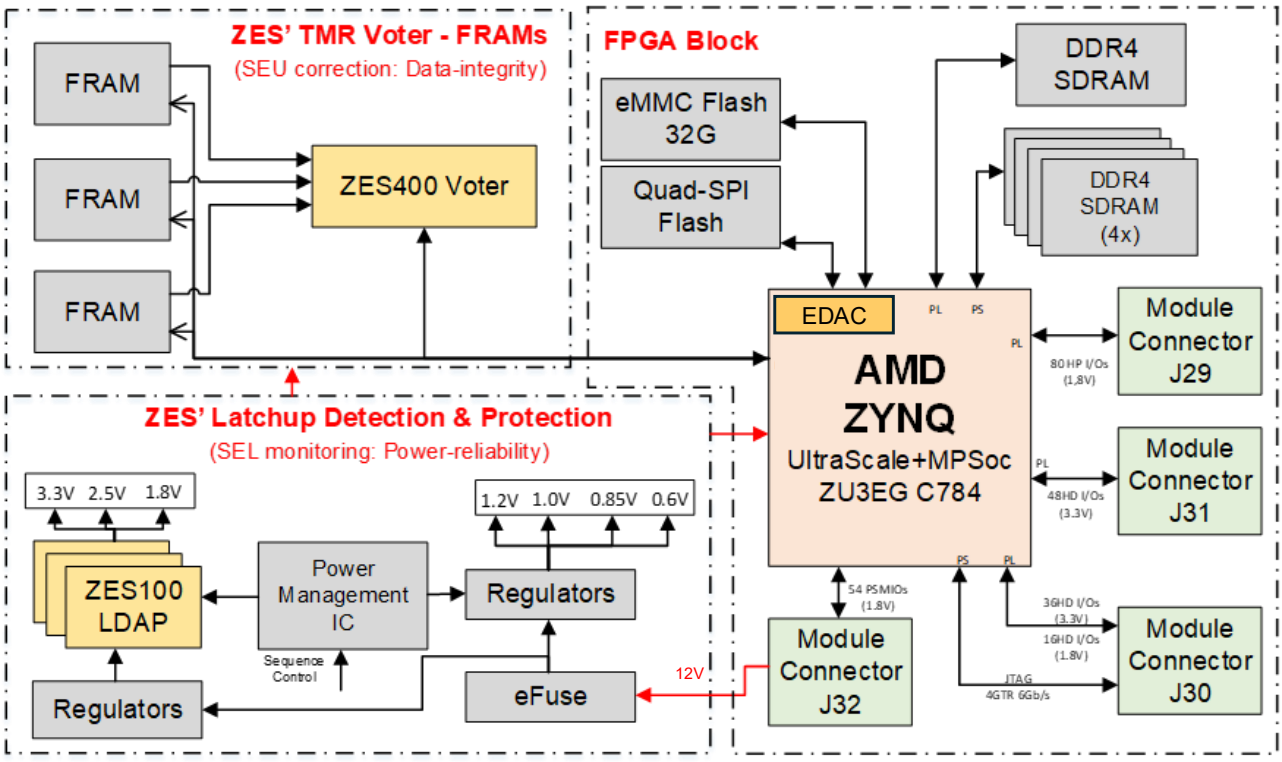

Figure 1: The simplified block diagram of ZSOM™-F01

4 Hardware Layout, Connectors, and Pin Out

4.1 Top and Bottom Views

- Top View (Figure 2): Displaying the placement of the Zynq MPSoC FPGA chip, DDR4 memory chips, QSPI flash, eMMC flash, clock components, LEDs, and power connectors.

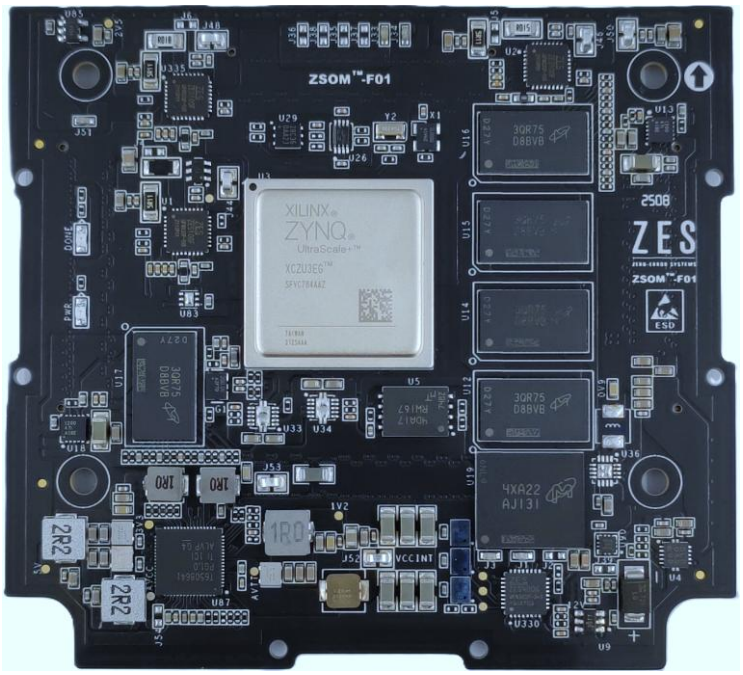

Figure 2: Top View

- Bottom View (Figure 3): Showing the four 120-pin board-to-board expansion connectors (J29–J32) along with mounting holes and additional passive components.

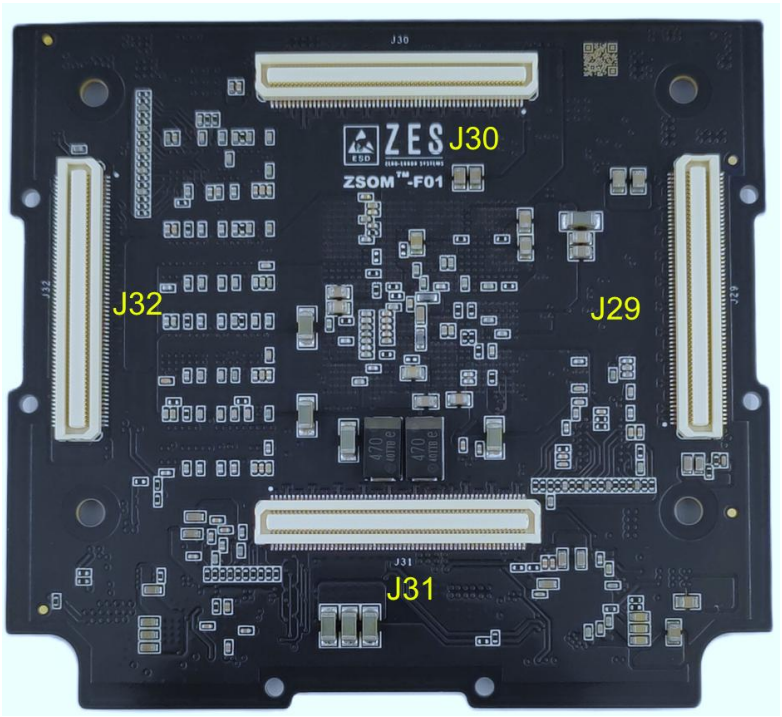

Figure 3: Bottom View

4.2 Board-to-Board Connectors

- Four high-speed 120-pin connectors facilitate interfacing with a base/carrier board. They provide access to:
  - PS I/O (including USB2.0, Gigabit Ethernet, SD Card interfaces, etc.)
  - High-speed transceiver channels (MGT) for extended communication links
  - PL I/O ports for custom peripheral connections
- The part number for the bottom connectors J29, J30, J31, and J32 on ZSOM-F01 is **Panasonic AXK5A2137YG.**
- The part number for mating the bottom connectors J1, J2, J3, and J4 on Carrier board ZSOM-F01-T01 is **Panasonic AXK6A2337YG**.

4.2.1 Connector J29

Pin name	Signal name	Pin name on MPSoC	Pin Description
1	B65_L2_N	V9	High Performance IO at Bank# 65
2	B65_L22_P	K8	High Performance IO at Bank# 65
3	B65_L2_P	U9	High Performance IO at Bank# 65
4	B65_L22_N	K7	High Performance IO at Bank# 65
5	GND	-	Ground
6	GND	-	Ground
7	B65_L4_N	T8	High Performance IO at Bank# 65
8	B65_L20_P	J6	High Performance IO at Bank# 65
9	B65_L4_P	R8	High Performance IO at Bank# 65
10	B65_L20_N	H6	High Performance IO at Bank# 65
11	GND	-	Ground
12	GND	-	Ground
13	B65_L1_N	Y8	High Performance IO at Bank# 65
14	B65_L6_N	T6	High Performance IO at Bank# 65
15	B65_L1_P	W8	High Performance IO at Bank# 65
16	B65_L6_P	R6	High Performance IO at Bank# 65
17	GND	-	Ground
18	GND	-	Ground
19	B65_L7_P	L1	High Performance IO at Bank# 65
20	B65_L17_P	N9	High Performance IO at Bank# 65
21	B65_L7_N	K1	High Performance IO at Bank# 65
22	B65_L17_N	N8	High Performance IO at Bank# 65
23	GND	-	Ground
24	GND	-	Ground
25	B65_L15_P	N7	High Performance IO at Bank# 65
26	B65_L9_P	K2	High Performance IO at Bank# 65
27	B65_L15_N	N6	High Performance IO at Bank# 65
28	B65_L9_N	J2	High Performance IO at Bank# 65
29	GND	-	Ground
30	GND	-	Ground
31	B65_L16_P	P7	High Performance IO at Bank# 65
32	B65_L3_N	V8	High Performance IO at Bank# 65
33	B65_L16_N	P6	High Performance IO at Bank# 65
34	B65_L3_P	U8	High Performance IO at Bank# 65
35	GND	-	Ground
36	GND	-	Ground
37	B65_L14_P	M6	High Performance IO at Bank# 65
38	B65_L19_P	J5	High Performance IO at Bank# 65
39	B65_L14_N	L5	High Performance IO at Bank# 65
40	B65_L19_N	J4	High Performance IO at Bank# 65
41	GND	-	Ground
42	GND	-	Ground
43	B65_L5_N	T7	High Performance IO at Bank# 65
44	B65_L18_P	M8	High Performance IO at Bank# 65
45	B65_L5_P	R7	High Performance IO at Bank# 65
46	B65_L18_N	L8	High Performance IO at Bank# 65
47	GND	-	Ground
48	GND	-	Ground
49	B65_L11_N	K3	High Performance IO at Bank# 65
50	B65_L8_P	J1	High Performance IO at Bank# 65
51	B65_L11_P	K4	High Performance IO at Bank# 65
52	B65_L8_N	H1	High Performance IO at Bank# 65
53	GND	-	Ground

54	GND	-	Ground
55	B65_L10_N	H3	High Performance IO at Bank# 65
56	B65_L24_N	H8	High Performance IO at Bank# 65
57	B65_L10_P	H4	High Performance IO at Bank# 65
58	B65_L24_P	H9	High Performance IO at Bank# 65
59	GND	-	Ground
60	GND	-	Ground
61	B66_L3_P	F2	High Performance IO at Bank# 66
62	B65_L12_P	L3	High Performance IO at Bank# 65
63	B66_L3_N	E2	High Performance IO at Bank# 66
64	B65_L12_N	L2	High Performance IO at Bank# 65
65	GND	-	Ground
66	GND	-	Ground
67	B66_L1_P	G1	High Performance IO at Bank# 66
68	B65_L13_N	L6	High Performance IO at Bank# 65
69	B66_L1_N	F1	High Performance IO at Bank# 66
70	B65_L13_P	L7	High Performance IO at Bank# 65
71	GND	-	Ground
72	GND	-	Ground
73	B66_L6_P	G5	High Performance IO at Bank# 66
74	B65_L21_P	J7	High Performance IO at Bank# 65
75	B66_L6_N	F5	High Performance IO at Bank# 66
76	B65_L21_N	H7	High Performance IO at Bank# 65
77	GND	-	Ground
78	GND	-	Ground
79	B66_L16_P	G8	High Performance IO at Bank# 66
80	B65_L23_P	K9	High Performance IO at Bank# 65
81	B66_L16_N	F7	High Performance IO at Bank# 66
82	B65_L23_N	J9	High Performance IO at Bank# 65
83	GND	-	Ground
84	GND	-	Ground
85	B66_L15_P	G6	High Performance IO at Bank# 66
86	B66_L5_N	E3	High Performance IO at Bank# 66
87	B66_L15_N	F6	High Performance IO at Bank# 66
88	B66_L5_P	E4	High Performance IO at Bank# 66
89	GND	-	Ground
90	GND	-	Ground
91	B66_L4_P	G3	High Performance IO at Bank# 66
92	B66_L2_P	E1	High Performance IO at Bank# 66
93	B66_L4_N	F3	High Performance IO at Bank# 66
94	B66_L2_N	D1	High Performance IO at Bank# 66
95	GND	-	Ground
96	GND	-	Ground
97	B66_L11_P	D4	High Performance IO at Bank# 66
98	B66_L20_P	C6	High Performance IO at Bank# 66
99	B66_L11_N	C4	High Performance IO at Bank# 66
100	B66_L20_N	B6	High Performance IO at Bank# 66
101	GND	-	Ground
102	GND	-	Ground
103	B66_L12_P	C3	High Performance IO at Bank# 66
104	B66_L7_P	C1	High Performance IO at Bank# 66
105	B66_L12_N	C2	High Performance IO at Bank# 66
106	B66_L7_N	B1	High Performance IO at Bank# 66
107	GND	-	Ground
108	GND	-	Ground
109	B66_L13_N	D6	High Performance IO at Bank# 66
110	B66_L10_P	B4	High Performance IO at Bank# 66
111	B66_L13_P	D7	High Performance IO at Bank# 66

112	B66_L10_N	A4	High Performance IO at Bank# 66
113	GND	-	Ground
114	GND	-	Ground
115	B66_L8_N	A1	High Performance IO at Bank# 66
116	B66_L9_P	B3	High Performance IO at Bank# 66
117	B66_L8_P	A2	High Performance IO at Bank# 66
118	B66_L9_N	A3	High Performance IO at Bank# 66
119	GND	-	Ground
120	GND	-	Ground

4.2.2 Connector J30

Pin name	Signal name	Pin name on MPSoC	Pin Description
1	B66_L14_P	E5	High Performance IO at Bank# 66
2	FPGA_TDI	R18	PS Configuration JTAG Test Data In pin at Bank# 503
3	B66_L14_N	D5	High Performance IO at Bank# 66
4	FPGA_TCK	R19	PS Configuration JTAG Test Clock pin at Bank# 503
5	GND	-	Ground
6	GND	-	Ground
7	B66_L22_P	C8	High Performance IO at Bank# 66
8	FPGA_TDO	T21	PS Configuration JTAG Test Data Out pin at Bank# 503
9	B66_L22_N	B8	High Performance IO at Bank# 66
10	FPGA_TMS	N21	PS Configuration JTAG Test Mode Select In pin at Bank# 503
11	GND	-	Ground
12	GND	-	Ground
13	B66_L19_N	A5	High Performance IO at Bank# 66
14	B66_L21_N	A6	High Performance IO at Bank# 66
15	B66_L19_P	B5	High Performance IO at Bank# 66
16	B66_L21_P	A7	High Performance IO at Bank# 66
17	GND	-	Ground
18	GND	-	Ground
19	B66_L24_P	C9	High Performance IO at Bank# 66
20	B66_L17_P	F8	High Performance IO at Bank# 66
21	B66_L24_N	B9	High Performance IO at Bank# 66
22	B66_L17_N	E8	High Performance IO at Bank# 66
23	GND	-	Ground
24	GND	-	Ground
25	B66_L23_N	A8	High Performance IO at Bank# 66
26	B45_L9_P	C11	High Density IO at Bank# 25
27	B66_L23_P	A9	High Performance IO at Bank# 66
28	B45_L9_N	B10	High Density IO at Bank# 25
29	GND	-	Ground
30	GND	-	Ground
31	B45_L5_N	F10	High Density IO at Bank# 25
32	B45_L10_P	B11	High Density IO at Bank# 25
33	B45_L5_P	G11	High Density IO at Bank# 25
34	B45_L10_N	A10	High Density IO at Bank# 25
35	GND	-	Ground
36	GND	-	Ground
37	B66_L18_N	D9	High Performance IO at Bank# 66
38	B45_L12_P	D12	High Density IO at Bank# 25
39	B66_L18_P	E9	High Performance IO at Bank# 66
40	B45_L12_N	C12	High Density IO at Bank# 25
41	GND	-	Ground
42	GND	-	Ground
43	B45_L4_N	H12	High Density IO at Bank# 25
44	B45_L11_P	A12	High Density IO at Bank# 25
45	B45_L4_P	J12	High Density IO at Bank# 25
46	B45_L11_N	A11	High Density IO at Bank# 25
47	GND	-	Ground
48	GND	-	Ground
49	B46_L11_P	K14	High Density IO at Bank# 26
50	B45_L6_N	F11	High Density IO at Bank# 25

51	B46_L11_N	J14	High Density IO at Bank# 26
52	B45_L6_P	F12	High Density IO at Bank# 25
53	GND	-	Ground
54	GND	-	Ground
55	B46_L10_N	H13	High Density IO at Bank# 26
56	B46_L6_N	E13	High Density IO at Bank# 26
57	B46_L10_P	H14	High Density IO at Bank# 26
58	B46_L6_P	E14	High Density IO at Bank# 26
59	GND	-	Ground
60	GND	-	Ground
61	B46_L7_N	F13	High Density IO at Bank# 26
62	B46_L3_N	A13	High Density IO at Bank# 26
63	B46_L7_P	G13	High Density IO at Bank# 26
64	B46_L3_P	B13	High Density IO at Bank# 26
65	GND	-	Ground
66	GND	-	Ground
67	B46_L9_N	G14	High Density IO at Bank# 26
68	B46_L2_N	A14	High Density IO at Bank# 26
69	B46_L9_P	G15	High Density IO at Bank# 26
70	B46_L2_P	B14	High Density IO at Bank# 26
71	GND	-	Ground
72	GND	-	Ground
73	B46_L5_N	D14	High Density IO at Bank# 26
74	B46_L4_N	C13	High Density IO at Bank# 26
79	B46_L5_P	D15	High Density IO at Bank# 26
76	B46_L4_P	C14	High Density IO at Bank# 26
77	GND	-	Ground
78	GND	-	Ground
79	B46_L1_P	B15	High Density IO at Bank# 26
80	B46_L12_P	L14	High Density IO at Bank# 26
81	B46_L1_N	A15	High Density IO at Bank# 26
82	B46_L12_N	L13	High Density IO at Bank# 26
83	GND	-	Ground
84	GND	-	Ground
85	505_CLK2_P	C21	PS GigaTransceiver Clk Pin 2P at Bank# 505
86	505_CLK1_P	E21	PS GigaTransceiver Clk Pin 1P at Bank# 505
87	505_CLK2_N	C22	PS GigaTransceiver Clk Pin 2N at Bank# 505
88	505_CLK1_N	E22	PS GigaTransceiver Clk Pin 1N at Bank# 505
89	GND	-	Ground
90	GND	-	Ground
91	505_CLK0_P	F23	PS GigaTransceiver Clk Pin 0P at Bank# 505
92	505_CLK3_P	A21	PS GigaTransceiver Clk Pin 3P at Bank# 505
93	505_CLK0_N	F24	PS GigaTransceiver Clk Pin 0N at Bank# 505
94	505_CLK3_N	A22	PS GigaTransceiver Clk Pin 3N at Bank# 505
95	GND	-	Ground
96	GND	-	Ground
97	505_TX0_P	E25	PS GigaTransceiver TX Pin 0P at Bank# 505
98	505_TX3_P	B23	PS GigaTransceiver TX Pin 3P at Bank# 505
99	505_TX0_N	E26	PS GigaTransceiver TX Pin 0N at Bank# 505

100	505_TX3_N	B24	PS GigaTransceiver TX Pin 3N at Bank# 505
101	GND	-	Ground
102	GND	-	Ground
103	505_RX0_P	F27	PS GigaTransceiver RX Pin 0P at Bank# 505
104	505_RX3_P	A25	PS GigaTransceiver RX Pin 3P at Bank# 505
105	505_RX0_N	F28	PS GigaTransceiver RX Pin 0N at Bank# 505
106	505_RX3_N	A26	PS GigaTransceiver RX Pin 3N at Bank# 505
107	GND	-	Ground
108	GND	-	Ground
109	505_TX1_P	D23	PS GigaTransceiver TX Pin 1P at Bank# 505
110	505_TX2_P	C25	PS GigaTransceiver TX Pin 2P at Bank# 505
111	505_TX1_N	D24	PS GigaTransceiver TX Pin 1N at Bank# 505
112	505_TX2_N	C26	PS GigaTransceiver TX Pin 2N at Bank# 505
113	GND	-	Ground
114	GND	-	Ground
115	505_RX1_P	D27	PS GigaTransceiver RX Pin 1P at Bank# 505
116	505_RX2_P	B27	PS GigaTransceiver RX Pin 2P at Bank# 505
117	505_RX1_N	D28	PS GigaTransceiver RX Pin 1N at Bank# 505
118	505_RX2_N	B28	PS GigaTransceiver RX Pin 2N at Bank# 505
119	GND	-	Ground
120	GND	-	Ground

4.2.3 Connector J31

Pin name	Signal name	Pin name on MPSoC	Pin Description
1	B44_L10_P	Y14	High Density IO at Bank# 24
2	B44_L7_P	AA13	High Density IO at Bank# 24
3	B44_L10_N	Y13	High Density IO at Bank# 24
4	B44_L7_N	AB13	High Density IO at Bank# 24
5	GND	-	Ground
6	GND	-	Ground
7	B44_L6_P	AC14	High Density IO at Bank# 24
8	B43_L6_P	AC12	High Density IO at Bank# 44
9	B44_L6_N	AC13	High Density IO at Bank# 24
10	B43_L6_N	AD12	High Density IO at Bank# 44
11	GND	-	Ground
12	GND	-	Ground
13	B44_L5_P	AD15	High Density IO at Bank# 24
14	B43_L7_P	AD11	High Density IO at Bank# 44
15	B44_L5_N	AD14	High Density IO at Bank# 24
16	B43_L7_N	AD10	High Density IO at Bank# 44
17	GND	-	Ground
18	GND	-	Ground
19	B44_L1_P	AE15	High Density IO at Bank# 24
20	B43_L8_N	AC11	High Density IO at Bank# 44
21	B44_L1_N	AE14	High Density IO at Bank# 24
22	B43_L8_P	AB11	High Density IO at Bank# 44
23	GND	-	Ground
24	GND	-	Ground
25	B44_L12_P	Y12	High Density IO at Bank# 24
26	B44_L2_P	AG14	High Density IO at Bank# 24
27	B44_L12_N	AA12	High Density IO at Bank# 24
28	B44_L2_N	AH14	High Density IO at Bank# 24
29	GND	-	Ground
30	GND	-	Ground
31	B44_L3_P	AG13	High Density IO at Bank# 24
32	-	-	NC
33	B44_L3_N	AH13	High Density IO at Bank# 24
34	-	-	NC
35	GND	-	Ground
36	GND	-	Ground
37	B43_L12_N	AB9	High Density IO at Bank# 44
38	B43_L9_P	AA11	High Density IO at Bank# 44
39	B43_L12_P	AB10	High Density IO at Bank# 44
40	B43_L9_N	AA10	High Density IO at Bank# 44
41	GND	-	Ground
42	GND	-	Ground
43	B43_L10_N	Y10	High Density IO at Bank# 44
44	B43_L3_P	AH12	High Density IO at Bank# 44
45	B43_L10_P	W10	High Density IO at Bank# 44
46	B43_L3_N	AH11	High Density IO at Bank# 44
47	GND	-	Ground
48	GND	-	Ground
49	B44_L11_N	W11	High Density IO at Bank# 24
50	B43_L1_N	AH10	High Density IO at Bank# 44
51	B44_L11_P	W12	High Density IO at Bank# 24
52	B43_L1_P	AG10	High Density IO at Bank# 44
53	GND	-	Ground
54	GND	-	Ground

55	B44_L9_N	W13	High Density IO at Bank# 24
56	B44_L4_P	AE13	High Density IO at Bank# 24
57	B44_L9_P	W14	High Density IO at Bank# 24
58	B44_L4_N	AF13	High Density IO at Bank# 24
59	GND	-	Ground
60	GND	-	Ground
61	B44_L8_P	AB15	High Density IO at Bank# 24
62	B43_L5_P	AE12	High Density IO at Bank# 44
63	B44_L8_N	AB14	High Density IO at Bank# 24
64	B43_L5_N	AF12	High Density IO at Bank# 44
65	GND	-	Ground
66	GND	-	Ground
67	B43_L2_N	AG11	High Density IO at Bank# 44
68	B43_L4_P	AE10	High Density IO at Bank# 44
69	B43_L2_P	AF11	High Density IO at Bank# 44
70	B43_L4_N	AF10	High Density IO at Bank# 44
71	GND	-	Ground
72	GND	-	Ground
73	VBAT_IN	-	Battery power input for Real Time Clock (RTC).
74	B43_L11_P	Y9	High Density IO at Bank# 44
75	MR	-	Power Reset Key for PMIC from Carrier Board
76	B43_L11_N	AA8	High Density IO at Bank# 44
77	GND	-	Ground
78	GND	-	Ground
79	exRST	-	External reset input from the system
80	PS_POR_B	P16	PS Power On Reset Pin
81	MISO_E	H11	ZES400 Voter Error output, 3.3V CMOS voltage level
82	eFuse_PG	-	Power Good indication of eFuse. Digital output. This pin is an open-drain signal which is asserted high when the power FET has fully turned ON and is ready to deliver power.
83	GND	-	Ground
84	GND	-	Ground
85	eFuse_EN	-	Active high enable for the eFuse. It can be used to adjust the undervoltage lockout threshold. Analog input.
86	eFuse_FLT	-	Active low fault event indicator of eFuse. Digital output. This pin is an open-drain signal which is pulled low when a fault is detected.
87	eFuse_ENBar		Active low enable for the eFuse. It can be used to adjust the overvoltage lockout threshold. Analog input.
88	-	-	NC
89	GND	-	Ground
90	GND	-	Ground
91	224_CLK0_P	Y6	NC for 3EG, Reserved PIN for 4EV/5EV
92	224_CLK1_P	V6	NC for 3EG, Reserved PIN for 4EV/5EV
93	224_CLK0_N	Y5	NC for 3EG, Reserved PIN for 4EV/5EV
94	224_CLK1_N	V5	NC for 3EG, Reserved PIN for 4EV/5EV
95	GND	-	Ground
96	GND	-	Ground
97	224_TX3_N	N3	NC for 3EG, Reserved PIN for 4EV/5EV
98	224_RX3_N	P1	NC for 3EG, Reserved PIN for 4EV/5EV

99	224_TX3_P	N4	NC for 3EG, Reserved PIN for 4EV/5EV
100	224_RX3_P	P2	NC for 3EG, Reserved PIN for 4EV/5EV
101	GND	-	Ground
102	GND		Ground
103	224_TX2_N	R3	NC for 3EG, Reserved PIN for 4EV/5EV
104	224_RX2_N	T1	NC for 3EG, Reserved PIN for 4EV/5EV
105	224_TX2_P	R4	NC for 3EG, Reserved PIN for 4EV/5EV
106	224_RX2_P	T2	NC for 3EG, Reserved PIN for 4EV/5EV
107	GND		Ground
108	GND		Ground
109	224_TX1_N	U3	NC for 3EG, Reserved PIN for 4EV/5EV
110	224_RX1_N	V1	NC for 3EG, Reserved PIN for 4EV/5EV
111	224_TX1_P	U4	NC for 3EG, Reserved PIN for 4EV/5EV
112	224_RX1_P	V2	NC for 3EG, Reserved PIN for 4EV/5EV
113	GND	-	Ground
114	GND	-	Ground
115	224_TX0_N	W3	NC for 3EG, Reserved PIN for 4EV/5EV
116	224_RX0_N	Y1	NC for 3EG, Reserved PIN for 4EV/5EV
117	224_TX0_P	W4	NC for 3EG, Reserved PIN for 4EV/5EV
118	224_RX0_P	Y2	NC for 3EG, Reserved PIN for 4EV/5EV
119	GND	-	Ground
120	GND	-	Ground

4.2.4 Connector J32

Pin name	Signal name	Pin name on MPSoC	Pin Description
1	PS_MIO35	H17	PS Multiplexed IO 35 at Bank# 501
2	PS_MIO30	F16	PS Multiplexed IO 30 at Bank# 501
3	PS_MIO29	G16	PS Multiplexed IO 29 at Bank# 501
4	PS_MIO31	H16	PS Multiplexed IO 31 at Bank# 501
5	GND	-	Ground
6	GND	-	Ground
7	ex_Power_OFF	-	External Power-off forced by external system control when the three ZES100 LDAPs triggered repeatedly
8	PS_MIO58	F18	PS Multiplexed IO 58 at Bank# 501
9	gRST	-	Global reset for PMIC, active by low, Digital input.
10	PS_MIO53	D16	PS Multiplexed IO 53 at Bank# 501
11	GND	-	Ground
12	GND	-	Ground
13	PS_MODE0	P19	PS Configuration Mode pin 0 at Bank# 503
14	PS_MIO52	G18	PS Multiplexed IO 52 at Bank# 502
15	PS_MODE1	P20	PS Configuration Mode pin 1 at Bank# 503
16	PS_MIO55	B16	PS Multiplexed IO 55 at Bank# 502
17	GND	-	Ground
18	GND	-	Ground
19	PS_MODE2	R20	PS Configuration Mode pin 2 at Bank# 503
20	PS_MIO56	C16	PS Multiplexed IO 56 at Bank# 502
21	PS_MODE3	T20	PS Configuration Mode pin 3 at Bank# 503
22	PS_MIO57	A16	PS Multiplexed IO 57 at Bank# 502
23	GND	-	Ground
24	GND	-	Ground
25	PS_MIO36	K17	PS Multiplexed IO 36 at Bank# 501
26	PS_MIO54	F17	PS Multiplexed IO 54 at Bank# 502
27	PS_MIO37	J17	PS Multiplexed IO 37 at Bank# 501
28	PS_MIO27	J15	PS Multiplexed IO 27 at Bank# 501
29	GND	-	Ground
30	GND	-	Ground
31	-	-	NC
32	PS_MIO28	K15	PS Multiplexed IO 28 at Bank# 501
33	PS_MIO77	F20	PS Multiplexed IO 77 at Bank# 502
34	PS_MIO59	E17	PS Multiplexed IO 59 at Bank# 502
35	GND	-	Ground
36	GND	-	Ground
37	PS_MIO76	B20	PS Multiplexed IO 76 at Bank# 502
38	PS_MIO60	C17	PS Multiplexed IO 60 at Bank# 502
39	-	-	NC
40	PS_MIO61	D17	PS Multiplexed IO 61 at Bank# 502
41	GND	-	Ground
42	GND	-	Ground
43	PS_MIO39	H19	PS Multiplexed IO 39 at Bank# 501
44	PS_MIO62	A17	PS Multiplexed IO 62 at Bank# 502
45	PS_MIO38	H18	PS Multiplexed IO 38 at Bank# 501
46	PS_MIO63	E18	PS Multiplexed IO 63 at Bank# 502
47	GND	-	Ground
48	GND	-	Ground
49	-	-	NC
50	PS_MIO65	A18	PS Multiplexed IO 65 at Bank# 502
51	PS_MIO40	K18	PS Multiplexed IO 40 at Bank# 501

52	PS_MIO66	G19	PS Multiplexed IO 66 at Bank# 502
53	GND	-	Ground
54	GND	-	Ground
55	PS_MIO44	J20	PS Multiplexed IO 44 at Bank# 501
56	PS_MIO67	B18	PS Multiplexed IO 67 at Bank# 502
57	PS_MIO45	K20	PS Multiplexed IO 45 at Bank# 501
58	PS_MIO68	C18	PS Multiplexed IO 68 at Bank# 502
59	GND	-	Ground
60	GND	-	Ground
61	PS_MIO47	H21	PS Multiplexed IO 47 at Bank# 501
62	PS_MIO64	E19	PS Multiplexed IO 64 at Bank# 502
63	PS_MIO48	J21	PS Multiplexed IO 48 at Bank# 501
64	PS_MIO69	D19	PS Multiplexed IO 69 at Bank# 502
65	GND	-	Ground
66	GND	-	Ground
67	PS_MIO41	J19	PS Multiplexed IO 41 at Bank# 501
68	PS_MIO74	D20	PS Multiplexed IO 74 at Bank# 502
69	PS_MIO32	J16	PS Multiplexed IO 32 at Bank# 501
70	PS_MIO73	G21	PS Multiplexed IO 73 at Bank# 502
71	GND	-	Ground
72	GND	-	Ground
73	PS_MIO46	L20	PS Multiplexed IO 46 at Bank# 501
74	PS_MIO72	G20	PS Multiplexed IO 72 at Bank# 502
75	PS_MIO50	M19	PS Multiplexed IO 50 at Bank# 501
76	PS_MIO71	B19	PS Multiplexed IO 71 at Bank# 502
77	GND	-	Ground
78	GND	-	Ground
79	PS_MIO49	M18	PS Multiplexed IO 49 at Bank# 501
80	PS_MIO75	A19	PS Multiplexed IO 75 at Bank# 502
81	PS_MIO34	L17	PS Multiplexed IO 34 at Bank# 501
82	PS_MIO70	C19	PS Multiplexed IO 70 at Bank# 502
83	GND	-	Ground
84	GND	-	Ground
85	PS_MIO26	L15	PS Multiplexed IO 26 at Bank# 501
86	PS_MIO43	K19	PS Multiplexed IO 43 at Bank# 501
87	PS_MIO24	AB19	PS Multiplexed IO 24 at Bank# 500
88	PS_MIO51	L21	PS Multiplexed IO 51 at Bank# 501
89	GND	-	Ground
90	GND	-	Ground
91	PS_MIO25	AB21	PS Multiplexed IO 25 at Bank# 500
92	PS_MIO42	L18	PS Multiplexed IO 42 at Bank# 501
93	-	-	NC
94	PS_MIO33	L16	PS Multiplexed IO 33 at Bank# 501
95	GND	-	Ground
96	GND	-	Ground
97	PG_3V3	-	3.3V Power supply to ZSOM-F01-T01 carrier board
98	-	-	NC
99	VCCO_65_CON	-	Power input for BANK65 from Carrier Board, <=1.8V
100	VCCO_66_CON	-	Power input for BANK66 from Carrier Board, <=1.8V
101	VCCO_65_CON	-	Power input for BANK65 from Carrier Board, <=1.8V
102	VCCO_66_CON	-	Power input for BANK66 from Carrier Board, <=1.8V
103	VCCO_65_CON	-	Power input for BANK65 from Carrier Board, <=1.8V

104	VCCO_66_CON	-	Power input for BANK66 from Carrier Board, <=1.8V
105	GND	-	Ground
106	GND	-	Ground
107	+12V	-	Power Supply, +12V from Carrier Board
108	+12V	-	Power Supply, +12V from Carrier Board
109	+12V	-	Power Supply, +12V from Carrier Board
110	+12V	-	Power Supply, +12V from Carrier Board
111	+12V	-	Power Supply, +12V from Carrier Board
112	+12V	-	Power Supply, +12V from Carrier Board
113	+12V	-	Power Supply, +12V from Carrier Board
114	+12V	-	Power Supply, +12V from Carrier Board
115	+12V	-	Power Supply, +12V from Carrier Board
116	+12V	-	Power Supply, +12V from Carrier Board
117	+12V	-	Power Supply, +12V from Carrier Board
118	+12V	-	Power Supply, +12V from Carrier Board
119	+12V	-	Power Supply, +12V from Carrier Board
120	+12V	-	Power Supply, +12V from Carrier Board

5 Technical Specifications

5.1 Electrical Characteristics

5.1.1 Nominal Operating Characteristics

Table 1: Nominal Operating Characteristics

No	Parameters	Min	Typ	Max	Unit	Note
1	Power Supply Voltage	6	12	16	V	
2	PS Core Voltage (VCC_PS)	0.85	0.85	0.87	V	AMD Zynq UltraScale+ Specification
3	PL Core Voltage (VCC_PL)	0.85	0.85	0.87	V	AMD Zynq UltraScale+ Specification
4	I/O Input Voltage (HP I/O)	1.71	1.8	1.89	V	HP (High Performance) I/O banks
5	I/O Input Voltage (HD I/O)	3.0	3.3	3.6	V	HD (High Density) I/O banks
6	GT receiver and transmitter		-	1.1	V	Refer to AMD specifications
7	Voltage on JTAG pin		3.3	3.4	V	Refer to AMD specifications

5.2 Power Consumption

No	Parameters	Value	Unit	Note
1	Power Supply Voltage	12	V	
2	Nominal Current	500	mA	
3	Peak Current	600	mA	

5.3 Operating Temperature Ranges

The operating temperature is between -30°C to 60°C in vacuum condition. The module operating temperature also depends on the shielding-case and heat-dissipation solution.

5.4 Mechanical Characteristics

5.4.1 Physical Properties

Table 2: Physical Properties of ZSOM-F01 without casing

	Unit	Value
Size	mm	81.69 x 90.17 x 6.83
Mass	grams	42

Table 3: Physical Properties of ZSOM-F01 with casing

	Unit	Value
Size	mm	81.69 x 90.17 x 9.90
Mass	grams	113

5.4.2 Mechanical Drawing

- The board is rectangular shape with dimension of 81.69 mm x 90.17 mm and thickness of 1.57 mm (standard PCB FR4 thickness).
- The four central holes (4- Φ 3.0) are for mounting the heat sink/shielding enclosure and the carrier board.
- The six holes along the edges (6- Φ 2.0) are also for mounting with heat sink/shielding enclosure.

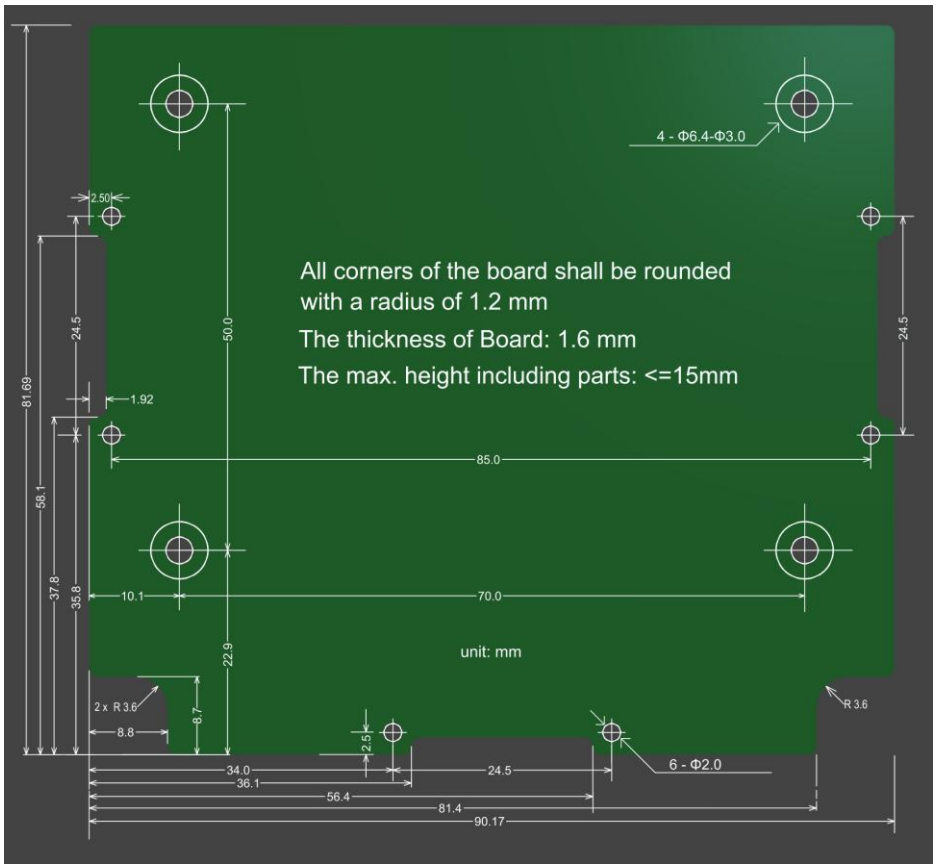

Figure 4: Board Dimension

The ZSOM™-F01 board has a total of four high-speed expansion ports (J29, J30, J31, J32). The dimensions of the connectors show on the Figure 5.

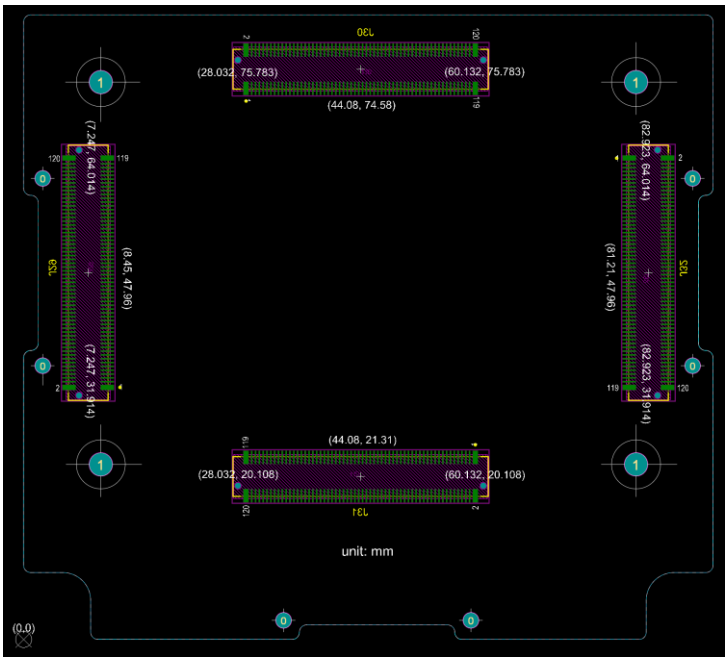

Figure 5: Board-to-Board Connector Dimensions

5.4.3 Casing Heat Sink

An Aluminium 7075 shielding/heat sink case is designed to mate with the ZSOM™-F01 board for the purposes of radiation-enhanced protection and heat sink. Figure 6 (a) and (b) depict the top view and bottom view of the casing, respectively.

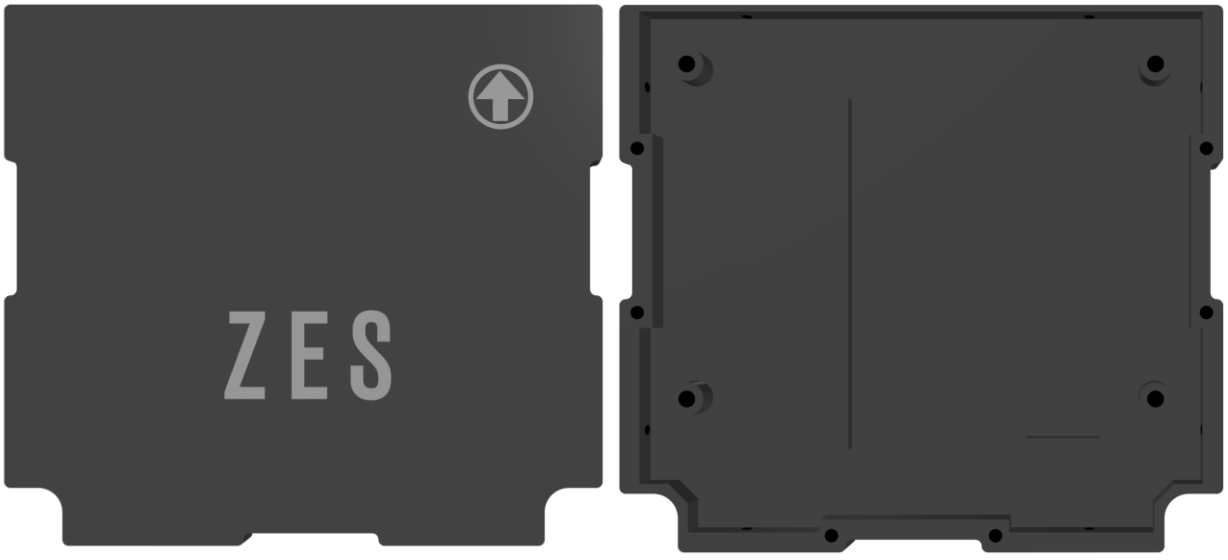

Figure 6: (a) Top view, and (b) Bottom view of the casing

Figure 7 (a) and (b) respectively depict the height of the casing and the cross-section view when the PCB board and the casing are mated.

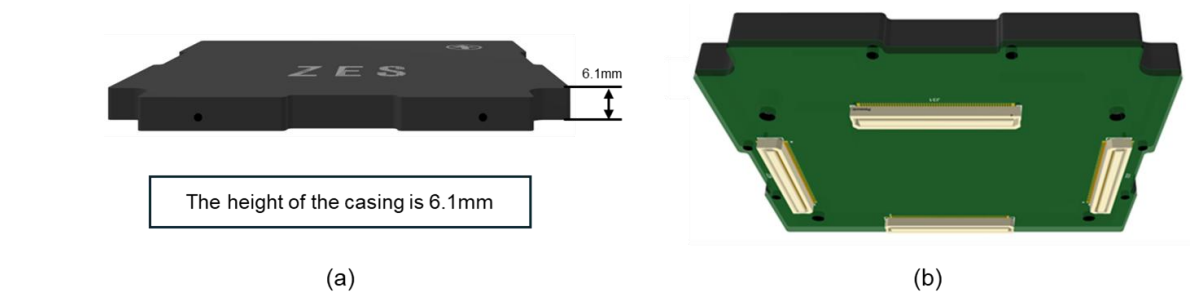

Figure 7: (a) Height of the casing, and (b) PCB and the casing are mated

5.4.4 PC104 Integration

The **ZSOM™-F01** board adheres to the **PC104** and **CubeSat specifications (see Figure 8),** allowing seamless integration into embedded systems, especially for ultra small form factor **Space payload applications.**

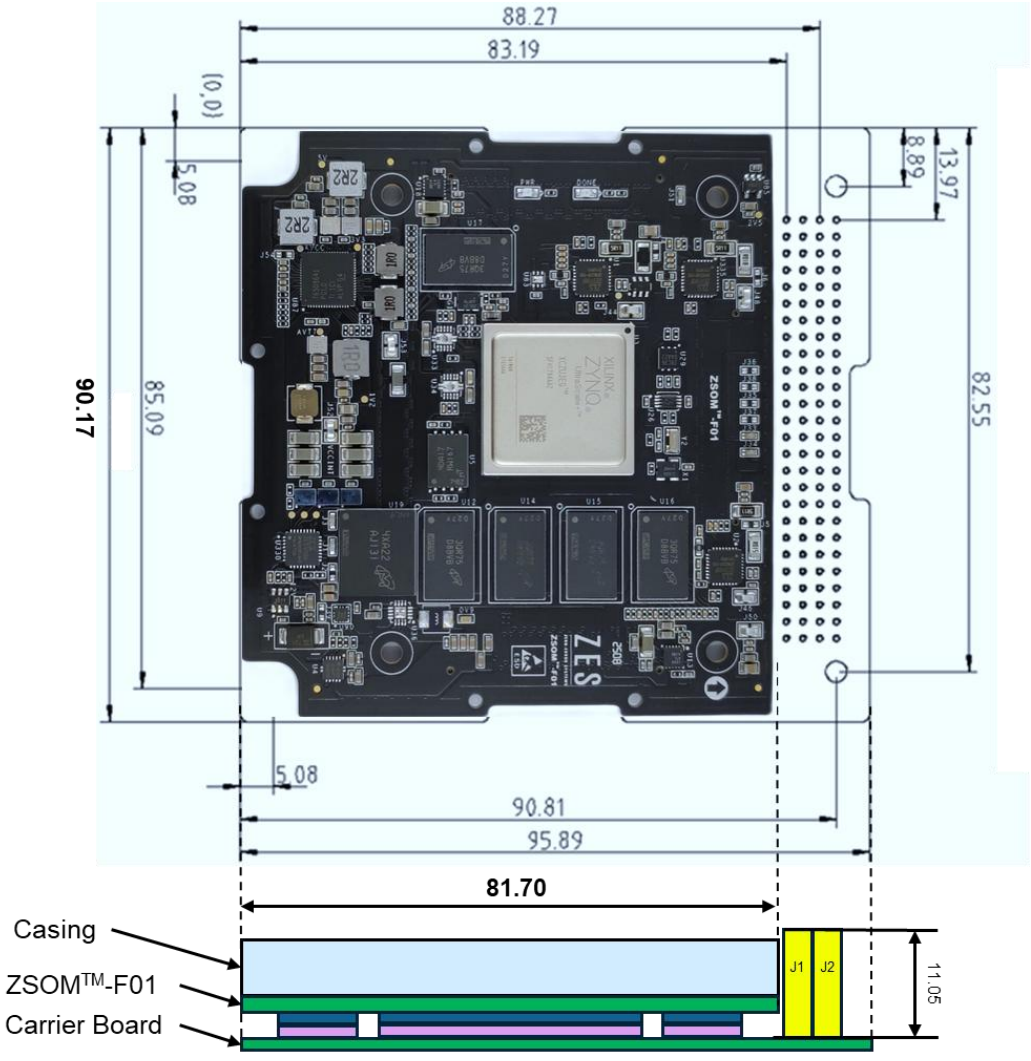

Figure 8: ZSOM™-F01 Integrated to Carrier board (PC104 standard)

6 Evaluation Carrier Board (EVK) for Ground Testing

The evaluation carrier board ZSOM™-F01-T01 is available to connect the ZSOM™-F01 for an application development and/or debugging/testing. The integration between the evaluation carrier board and the ZSOM™-F01 is based on the B2B connectors at the bottom of the PCB.

The evaluation carrier board provides all the necessary interfaces to support the functional tests of the module ZSOM™-F01. All the interfaces and connectors positions have been shown in Figure 9.

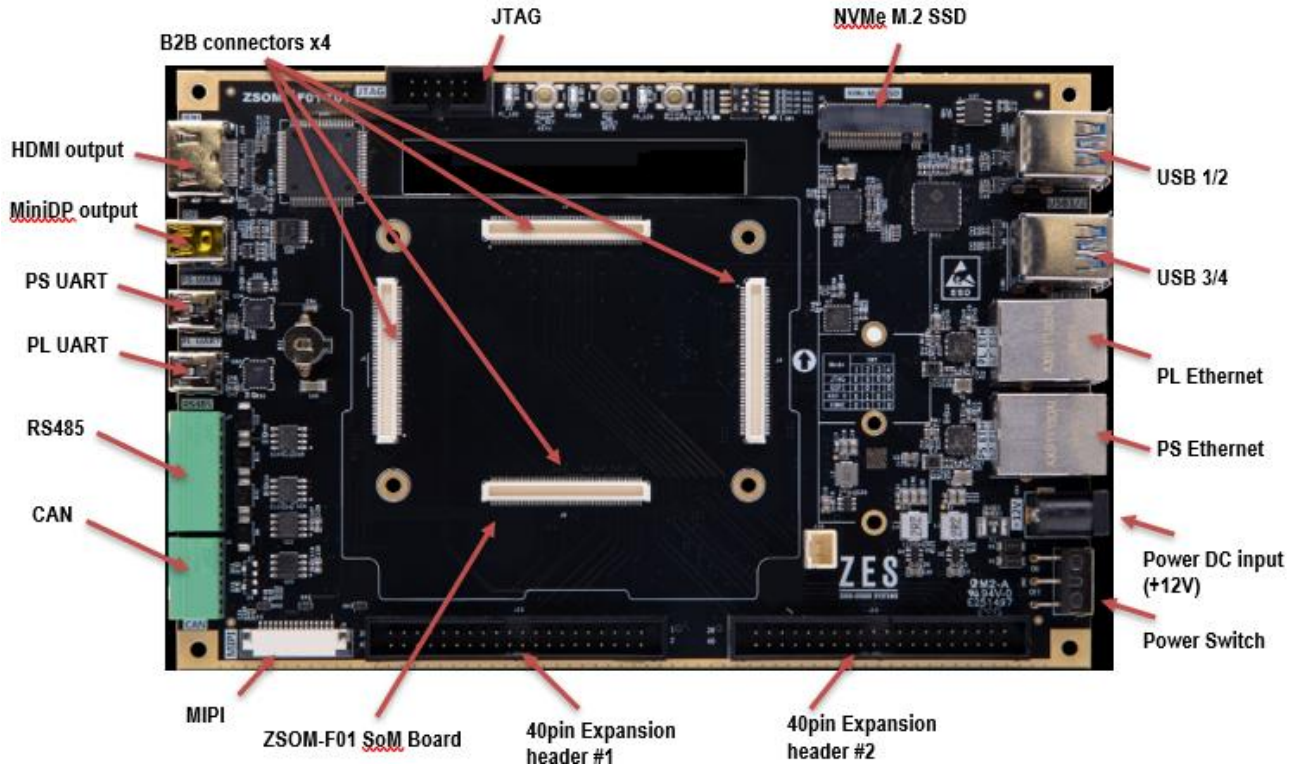

Figure 9: Evaluation Carrier Board Diagram

7 Data Protocol/Peripherals

7.1 I²C

The I²C communication pin assignments are as follows:

Table 4: I²C Pin Assignment

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
PS_IIC1_SCL	PS_MIO24	AB19	IIC Clock Singal
PS_IIC1_SDA	PS_MIO25	AB21	IIC Data Signal

7.2 RS485

The RS485 communication pin assignments are as follows:

Table 5: RS485 Pin Assignment

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
PL_485_TXD1	B43_L1_N	AH10	1st channel 485 Transmitter
PL_485_RXD1	B44_L4_P	AE13	1st channel 485 Receiver
PL_485_DE1	B45_L10_P	B11	1st channel 485 Transmit Enable
PL_485_TXD2	B43_L1_P	AG10	2nd channel 485 Transmitter
PL_485_RXD2	B44_L4_N	AF13	2nd channel 485 Receiver
PL_485_DE2	B45_L10_N	A10	2nd channel 485 Transmit Enable

7.3 CAN

The CAN communication pin assignments are as follows:

Table 6: CAN Pin Assignment

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
PS_CAN1_TX	PS_MIO32	J16	CAN1 Receiver
PS_CAN1_RX	PS_MIO33	L16	CAN1 Transmitter
PS_CAN2_TX	PS_MIO39	H19	CAN2 Receiver
PS_CAN2_RX	PS_MIO38	H18	CAN2 Transmitter

7.4 UART

The UART communication pin assignments are as follows:

Table 7: UART Pin Assignment

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
PS_UART0_TX	PS_MIO43	K19	PS UART Data Output
PS_UART0_RX	PS_MIO42	L18	PS UART Data Input
PL_UART_TX	B43_L3_P	AH12	PL UART Data Output
PL_UART_RX	B43_L3_N	AH11	PL UART Data Input

7.5 Gigabit Ethernet (GigE)

The Gigabit Ethernet communication pin assignments are as follows:

Table 8: Gigabit Ethernet Pin Assignment

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
PHY1_TXCK	PS_MIO64	E19	Ethernet 1 RGMII Transmit Clock
PHY1_TXD0	PS_MIO65	A18	Ethernet 1 Transmit data bit0
PHY1_TXD1	PS_MIO66	G19	Ethernet 1 Transmit data bit1
PHY1_TXD2	PS_MIO67	B18	Ethernet 1 Transmit data bit2
PHY1_TXD3	PS_MIO68	C18	Ethernet 1 Transmit data bit3
PHY1_TXCTL	PS_MIO69	D19	Ethernet 1 Transmit Enable Signal
PHY1_RXCK	PS_MIO70	C19	Ethernet 1 RGMII Receive Clock
PHY1_RXD0	PS_MIO71	B19	Ethernet 1 Receive Data Bit0
PHY1_RXD1	PS_MIO72	G20	Ethernet 1 Receive Data Bit1
PHY1_RXD2	PS_MIO73	G21	Ethernet 1 Receive Data Bit2
PHY1_RXD3	PS_MIO74	D20	Ethernet 1 Receive Data Bit3
PHY1_RXCTL	PS_MIO75	A19	Ethernet 1 Receive Enable Signal
PHY1_MDC	PS_MIO76	B20	Ethernet 1 MDIO Clock Management
PHY_MDIO	PS_MIO77	F20	Ethernet 1 MDIO Data Management
PHY2_TXCK	B66_L17_N	E8	Ethernet 2 RGMII Transmit Clock
PHY2_TXD0	B66_L18_P	E9	Ethernet 2 Transmit data bit0
PHY2_TXD1	B66_L18_N	D9	Ethernet 2 Transmit data bit1
PHY2_TXD2	B66_L23_P	A9	Ethernet 2 Transmit data bit2
PHY2_TXD3	B66_L23_N	A8	Ethernet 2 Transmit data bit3
PHY2_TXCTL	B66_L24_N	B9	Ethernet 2 Transmit Enable Signal
PHY2_RXCK	B66_L14_P	E5	Ethernet 2 RGMII Receive Clock
PHY2_RXD0	B66_L19_N	A5	Ethernet 2 Receive Data Bit0
PHY2_RXD1	B66_L19_N	B5	Ethernet 2 Receive Data Bit1
PHY2_RXD2	B66_L17_P	F8	Ethernet 2 Receive Data Bit2
PHY2_RXD3	B66_L24_P	C9	Ethernet 2 Receive Data Bit3
PHY2_RXCTL	B66_L22_N	B8	Ethernet 2 Receive Enable Signal
PHY2_MDC	B66_L21_N	A6	Ethernet 2 MDIO Clock Management
PHY2_MDIO	B66_L22_P	C8	Ethernet 2 MDIO Data Management
PHY2_RESET	B66_L14_N	D5	Ethernet 2 Reset Signal

7.6 PCIE2.0

The PCIE communication pin assignments are as follows:

Table 9: PCIE2.0 Pin Assignment

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
PCIE_TX_P	505_TX0_P	E25	PCIe Data Transmit Positive
PCIE_TX_N	505_TX0_N	E26	PCIe Data Transmit Negative
PCIE_RX_P	505_RX0_P	F27	PCIe Data Receive Positive
PCIE_RX_N	505_RX0_N	F28	PCIe Data Receive Negative
505_PCIE_REFCLK_P	505_CLK0_P	F23	PCIe Reference Clock Positive
505_PCIE_REFCLK_N	505_CLK0_N	F24	PCIe Reference Clock Negative
PCIE_RSTn_MIO37	PS_MIO37_501	J17	Reset Signal

7.7 USB 3.0

The USB communication pin assignments are as follows

Table 10: USB 3.0 Pin Assignment

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
USB_SSTXP	505_TX1_P	D23	USB 3.0 Data Transmit Positive
USB_SSTXN	505_TX0_N	D24	USB 3.0 Data Transmit Negative
USB_SSRXP	505_RX0_P	D27	USB 3.0 Data Receive Positive
USB_SSRXN	505_RX0_N	D28	USB 3.0 Data Receive Negative
USB_DATA0	PS_MIO46	C16	USB 2.0 Data Bit 0
USB_DATA1	PS_MIO57	A16	USB 2.0 Data Bit 1
USB_DATA2	PS_MIO54	F17	USB 2.0 Data Bit 2
USB_DATA3	PS_MIO59	E17	USB 2.0 Data Bit 3
USB_DATA4	PS_MIO60	C17	USB 2.0 Data Bit 4
USB_DATA5	PS_MIO61	D17	USB 2.0 Data Bit 5
USB_DATA6	PS_MIO62	A17	USB 2.0 Data Bit 6
USB_DATA7	PS_MIO63	E18	USB 2.0 Data Bit 7
USB_STP	PS_MIO58	F18	USB 2.0 Stop Signal
USB_DIR	PS_MIO53	D16	USB 2.0 Data Direction Signal
USB_CLK	PS_MIO52	G18	USB 2.0 Clock Signal
USB_NXT	PS_MIO55	B16	USB 2.0 Next Data Signal
USB_RESET_N	PS_MIO31	H16	USB 2.0 Reset Signal

8 Software/Programming

- **Boot and Firmware Storage:**
  The board supports multiple boot modes, including eMMC* (default), QSPI, and JTAG. Boot mode selection is controlled by hardware switches. Each boot medium requires proper formatting and partitioning to store boot files (BOOT.BIN, boot.scr, image.ub, rootfs). For detailed boot process and configuration, refer to AMD UG1137: Zynq UltraScale+ MPSoC Software Development Guide

- **Programming Environment:**
  The board supports development using Xilinx tools
  - Vivado (2020.1) for FPGA design
    - Download Link: https://www.xilinx.com/support/download/index.html/content/xilinx/en/downloadNav/vivado-design-tools/archive.html
  - Vitis (2020.1) for embedded software
    - Download Link: https://www.xilinx.com/support/download/index.html/content/xilinx/en/downloadNav/vitis/archive-vitis.html

- **Application Development:**
  Developers can leverage extensive peripheral interfaces (UART, USB, SD card, Ethernet, etc.) available on the PS and PL sides for customized high-performance applications.

*eMMC mode is preferred for Flight mode.

9 ZES SEL/SEU Protection Technology in ZSOM-F01

9.1 SEL Protection Technology

ZSOM-F01 embodies three ZES100 LDAP-ICs to protect the SEL-sensitive local power supplies, namely VCC_AUX_L @ 1.8V, DDR_2V5_L @ 2.5V, and VCC_3V3_L @ 3.3V. Figure 10 (a) depicts the simplified connection diagram of these three local power supplies. As VCC_AUX_L is expected to deliver > 500mA, a discrete PMOS is used together with an ZES100 LDAP-IC. Whereas DDR_2V5_L and VCC_3V3_L are delivering < 500mA, the ZES100 LDAP-ICs per se (i.e., without a need of discrete PMOS) are sufficient to deliver the current. Figure 10 (b) depicts the connection diagram how to power-cycle the ZSOM-F01 once an SEL is detected, i.e., triggered by the Power Good (PG) signals of ZES100 LDAP-ICs. This triggering is via the three voting channels (CH2, CH3 and CH4) of ZES400 Voter-IC. Particularly, the ZES400 Voter-IC will receive the PG signals of ZES100 LDAP-ICs, and trigger the global reset signal (gRST) to reset the PMIC and the connecting FPGA.

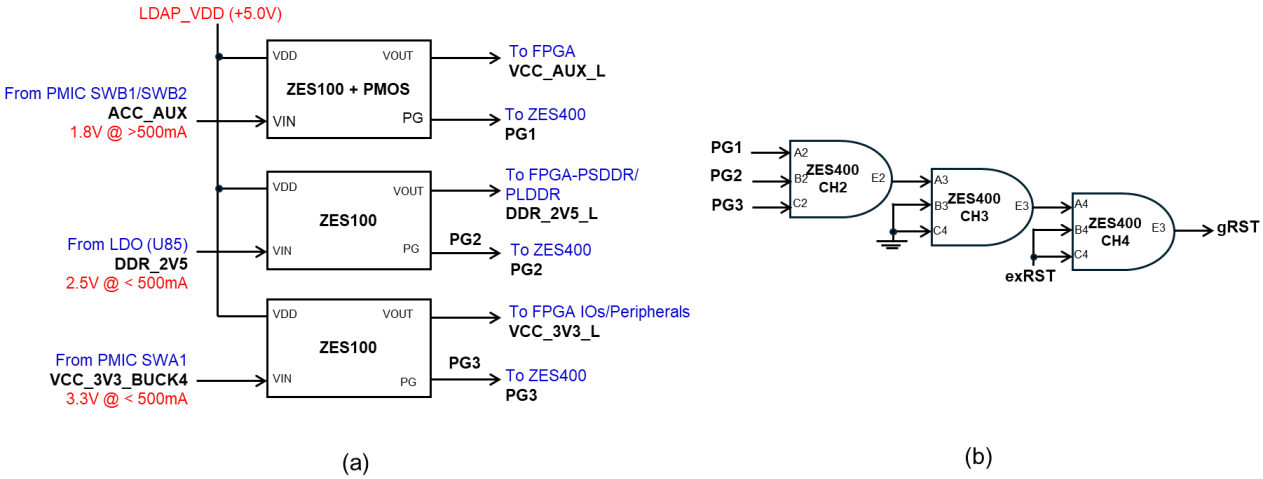

Figure 10: (a) Connection diagram of the three ZES100 LDAP-ICs for SEL detection/protection, (b) the reset mechanism via ZES400 Voter-IC

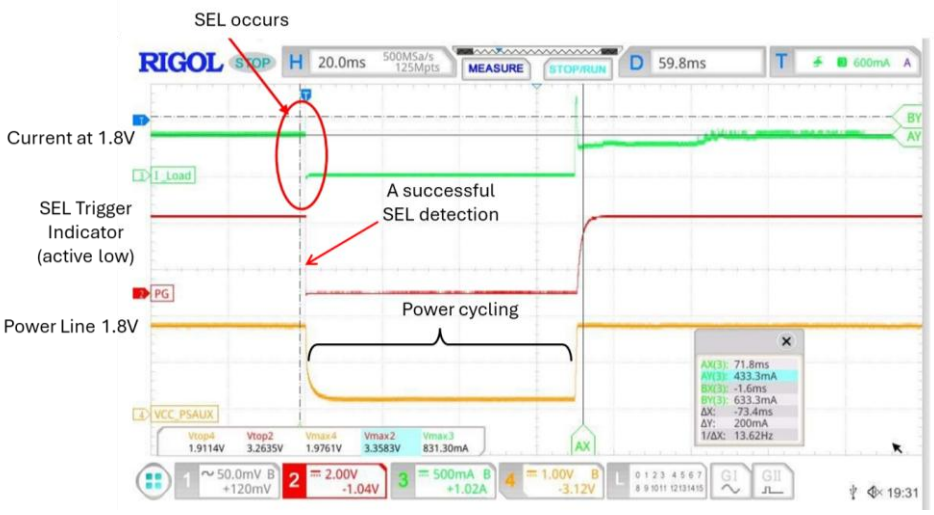

Figure 11: SEL triggering at VCC_AUX_L (1.8V)

9.2 SEU Protection Technology

ZSOM-F01 allows the ZES proprietary hardware-cum-software solution (i.e., ZES400 Voter-IC + FRAMs + EDAC) to protect data stored in memory blocks. Figure 12 depicts the simplified blocks how various memory

blocks are connected to the FPGA for EDAC code execution. Particularly, the ZES400 Voter-IC (and the associated TMR FRAMs) are physically connected to the FPGA via SPI interface ports. With the reconfigurability of FPGA, the SPI interface ports are configured to connect the PS side of the FPGA, so that the ARM core in the PS side can access the data at the TMR FRAMs. The PS side of the FPGA is further connected to the external memories including the eMMC (NAND) flash, QSPI (NOR) flash, and DDR4 memories. The PS side of the FPGA can also internally access the Block RAM (BRAM) of the FPGA. By using the ZES hardware-cum-software solution, the data stored in the eMMC flash, QSPI flash, DDR4 and BRAM can be checked against SEUs. If there is any SEUs, the errors (SEUs) can be recovered by ZES EDAC code. Please refer to the user guide for setting up the ZES EDAC code.

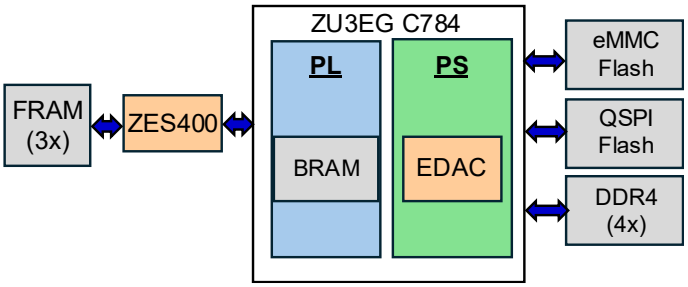

Figure 12: The simplified blocks how various memory blocks are connected to the FPGA for EDAC code execution

An image is stored inside the eMMC of the ZSOM-F01 and the data are protected by ZES EDAC code. Hypothetically the data are then randomly corrupted with 14 errors (14 bits flipped out of 50kB). The corrupted data would be recovered by the ZES EDAC. Figure 13 (a) – (c) depict the original picture, the corrupted picture with 14 bits flipped, and the corrected picture.

(a) (b) (c)

Figure 13: Data protection demonstration (picture data) in eMMC: (a) Original data, (b) Corrupted Data, and (c) Corrected data (with ZES EDAC)

10 Radiation and Environment Qualifications

ZSOM™-F01 is designed for operation in extreme environments, specifically tailored for Low Earth Orbit (LEO), Medium Earth Orbit (MEO), and Geostationary Earth Orbit (GEO). To ensure long-term reliability and robustness in space, the sample modules undergo extensive environmental testing in compliance with industry standards such as ECSS-E-ST-10-03, ECSS-Q-ST-70-38C, MIL-STD-883J, and NASA-STD-7001B.

These tests simulate the harsh radiation conditions that satellites and spaceborne electronics experience, including mechanical stress during launch, extreme temperature fluctuations, vacuum exposure, radiation effects, and electromagnetic interference (EMI/EMC) risks. ZSOM™-F01 is built to withstand these challenges while maintaining optimal performance.

Radiation and Environment Qualification tests are summarized as follows.

No	Category	Test Item	Condition	Remarks	Standard Reference
1	Radiation Test	Total Ionizing Dose (TID)	Cobalt-60 @ 15krad (Si)	10-year lifespan for LEO	MIL-STD-883J
2		Proton Test	Proton 80MeV @ fluence = $1.80*10^{10}$ #/cm^2 Proton 140MeV @ fluence = $7.6*10^{9}$ #/cm^2 Proton 200MeV @ fluence = $1.01*10^{10}$ #/cm^2	No SEL /hardware damage	JESD234, MIL-PRF-38535M
3	Thermal Test	Thermal Vacuum Test	Temperature range: -30°C to +60°C Pressure level: <1.0x 10^{-5} mbar Number of cycles: 4 cycles	Pass	ECSS-Q-ST-70-04C, ISO-19683
4		Test Stress Test	Temperature range: -35°C to 65°C Number of cycles: 24 cycles of low/high temperature	Pass	ECSS-Q-ST-70-08C, ISO-19683
5		Baking for Outgassing	Temperature: 85°C Pressure level: <1.0x 10^{-5} mbar Duration: 24 hours	Pass Total mass loss < 0.1%	NASA-STD-7002A
6	Mechanical Test	Sinusoidal Vibration	Frequency [Hz]: 5-8Hz – Level [G]: 20mm peak-peak Frequency [Hz]: 8-100Hz– Level [G]: 4.5G Sweep rate: 2 octaves per minute	Pass	ECSS-E-ST-10-03C, MIL-STD-7001B, MIL-STD-810H
7		Random Vibration	Overall: 14.1G RMS (Root Mean Square) Duration: 120 seconds on each axis	Pass	
8		Sine Burst	Frequency: 15Hz Cycles: 20 cycles Number of Burst: 10 Level: 12G	Pass	
9		Classical Shock Test	Peak Acceleration: 75G Pulse duration: 6ms	Pass	ECSS-E-ST-10-03C, MIL-STD-810H
10	Electrical Test	EMC	CS (Conducted Susceptibility) RS (Radiated Susceptibility)	Pass	ECSS-E-ST-20-07C, MIL-STD-461G
11		EMI	CE (Conducted Emissions) RE (Radiated Emissions)	Pass	

For detailed test results, please contact sales@zero-errorsystem.com

11 Revision History

Version	Description	Date
V0.1	Preliminary version	April-2025
V1.1	First version release	Aug-2025
V1.1a	Format update	Apr-2026

For the latest version of this document, please contact us sales@zero-errorsystem.com

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