Radiation Hardened Latching Current Limiter (LCL)- IC

Enabling Advanced Commercial-Off-The-Shelf (COTS) to 'Space-Grade'

Product Description

Semiconductor electronics in Space systems are prone to various anomaly, including Single Event Latch-Up (SEL) when exposed under radiation. These anomalies severely compromise the reliability of satellite systems and their mission lifetimes.

To enhance reliability, a current limiter microchip such as Latching Current Limiter (LCL) is typically adopted. By monitoring the supply current into an electronic system, the LCL disconnects the power to the electronic system when the supply current exceeds a preconfigured threshold.

LCL(28V) IC Part code 'ZES723LCL' is a Smart-LCL with primary functions are current limiter monitoring and power switching, and is a Radiation-Hardened LCL with wide input voltage range of 4V~28V DC, with integrated power transistors that can withstand up to 4A of output current, with very low quiescent current <2mA(typ.) and packaged in a compact plastic QFN48L.

ZES's Smart-LCL IC is designed based on ECSS-E-ST-20-20C, offering an unprecedented means in current limiter switching of the power supply lines. Specifically, ZES's Smart-LCL embodies a unique Smart-monitor with two types of operations: Latched or Re-triggerable, with built-in Smart current limitation for repetitive overloads, with Embedded current sense and Digital status for system monitoring. Further, to enable design flexibility LCL offers configurable trip-off and recovery times, configurable undervoltage protection, and Floating ground.

ZES' Smart-LCL is realized with Radiation Hardening By Design (RHBD) approach, hence highly immune towards various radiation effects in Space.

Target Applications

- Satellite's **Power switches (LCL)** for OBC, Payloads
- **Radiation hardened** and tolerant Power Distribution Units **(PDU)** and Electrical Power System (**EPS)**
- **Current Limiter Protection switches** for various subsystems

Key Features

- Wide-range supply voltage: 4V ~ 28V DC
- Output current up to 4A (internal transistors), or expandable using external MOSFETs
- External On and OFF commands with error tolerance
- Two types of operation: Latched or Re-triggerable
- Configurable trip-off and recovery times
- Smart current limitation for repetitive overload
- Embedded current sense
- Digital status for system monitoring
- Fast transient response with high loading inductance (e.g., 300uH)
- Configurable undervoltage protection
- Floating ground
- Space qualified technology
- Based on ECSS-E-ST-20-20C
- Radiation Hardened by Design (RHBD)
  TID: 75 krad (Si) HDR, LDR
  SEE: free up to xx MeV.cm^2/mg (TBC)
- Temp range operation (T_a = −40°C to +120°C)
- Qualified for Space Enhanced Plastic (SEP)
- ITAR free
- Package: QFN48L (9 x 9 x 0.75mm)

Electrical Performance

Input Voltage	4V to 28V
Maximum Output Current (integrated MOSFET)	4A
Quiescent Current	<2mA (Typ.)
Shut Down Current	< 0.2 mA

Radiation Performance (Cyclotron Verified)

TID	75 krad (Si)
LET	xx MeV-cm^2/mg (TBC)

(TBC: To be confirmed after testing)

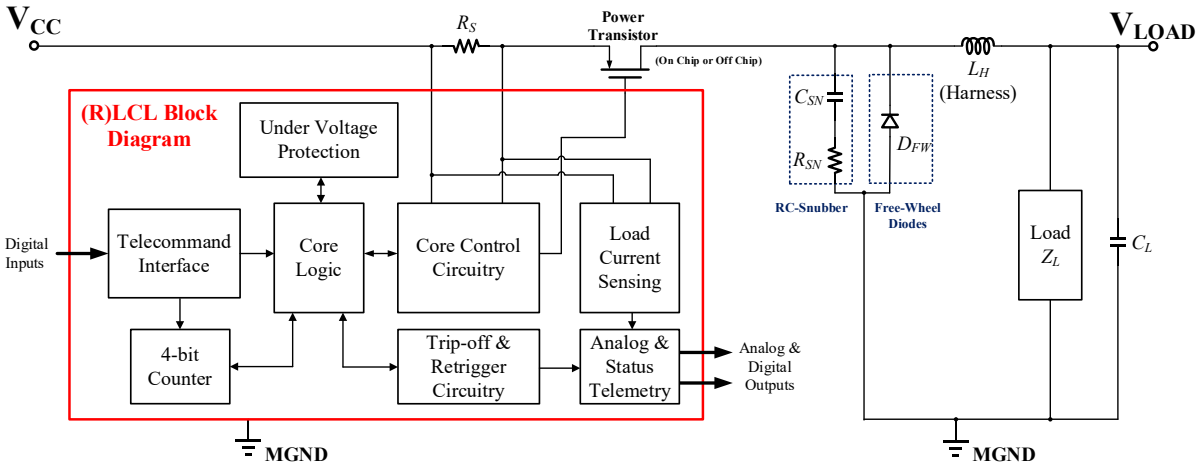
Ordering Information (Tentative Part code)

Part No.	Description	Grade	Form Factor	Size
ZES723LCLGQ-EP	ZES723 LCL 28V 4A Ground Model	GM*	QFN48L	9mm x 9mm
ZES723LCLFQ-EP	ZES723 LCL 28V 4A Flight Model	FM	QFN48L	9mm x 9mm
ZES723LCLGEV-EP	ZES723 LCL 28V 4A Evaluation Board	Eval. Kit	Evaluation Board	11cm x 11cm

For price, delivery, and ordering information please contact sales@zero-errorsystems.com

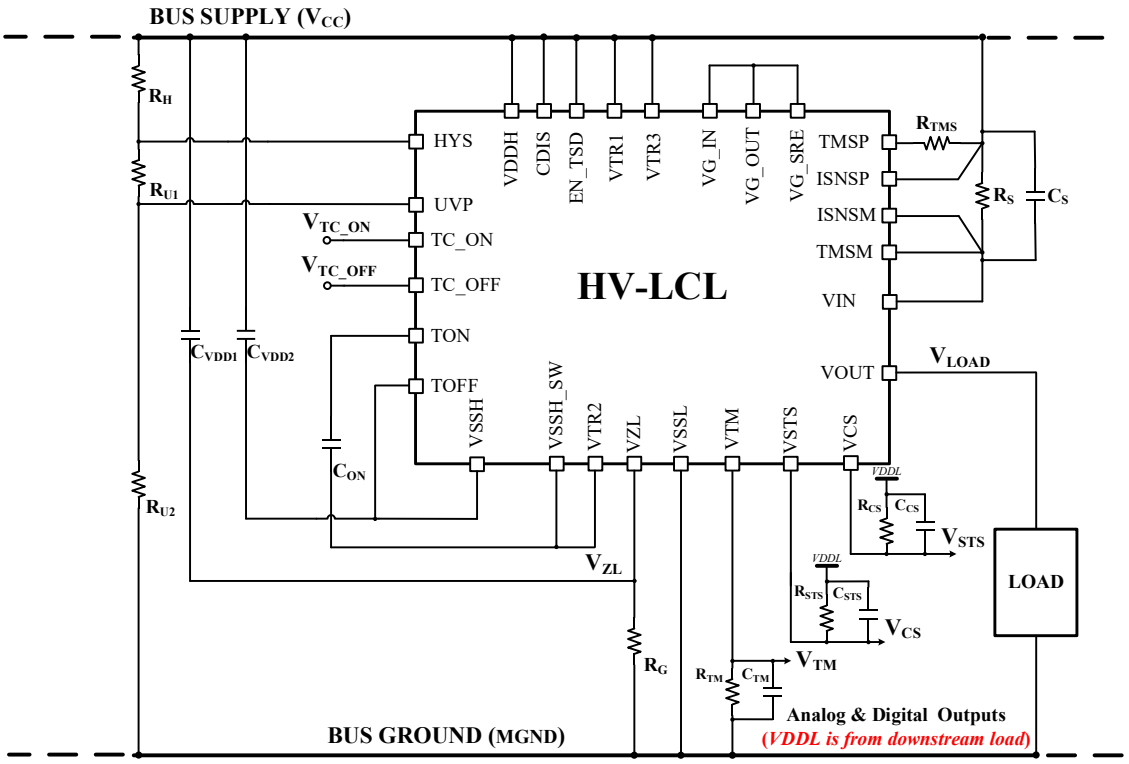
* Ground Model (GM) units are intended for engineering evaluation only. These units are not suitable for qualification, production, radiation testing or flight use. Parts are not warranted for performance over the full specified temperature range of –40°C to 120°C or operating life.

1. ZES723LCL Functional Block Diagram

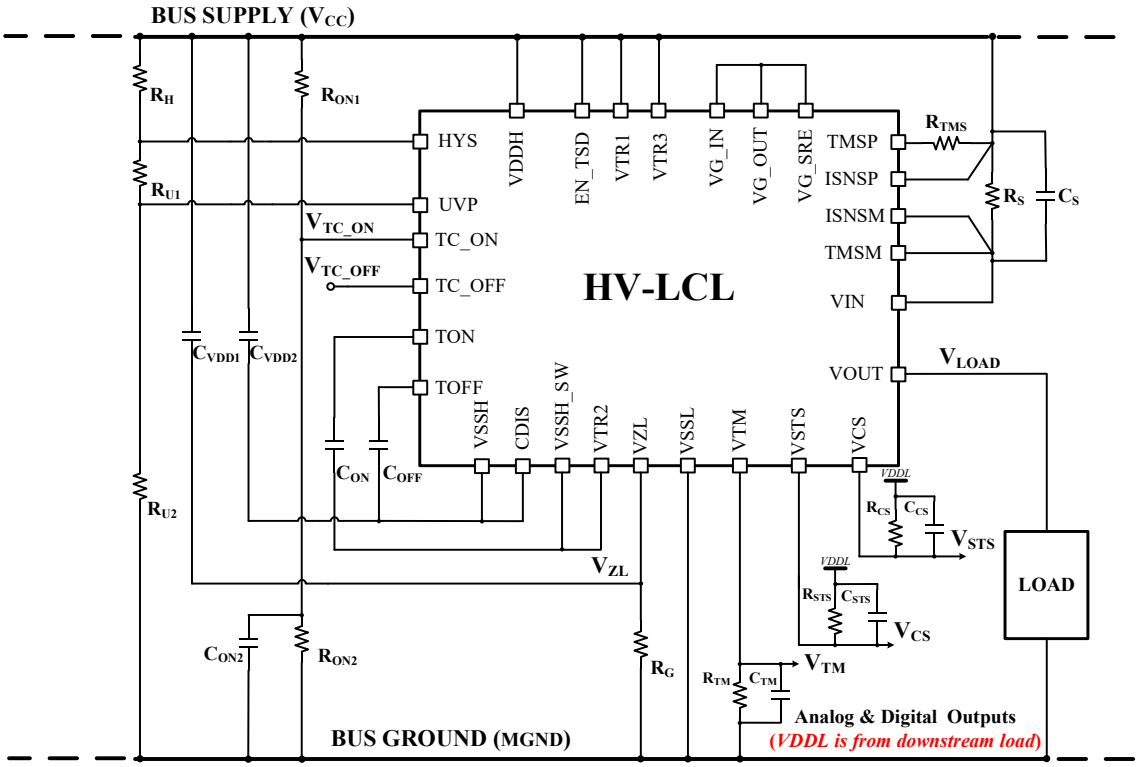


2. Typical Application Circuit

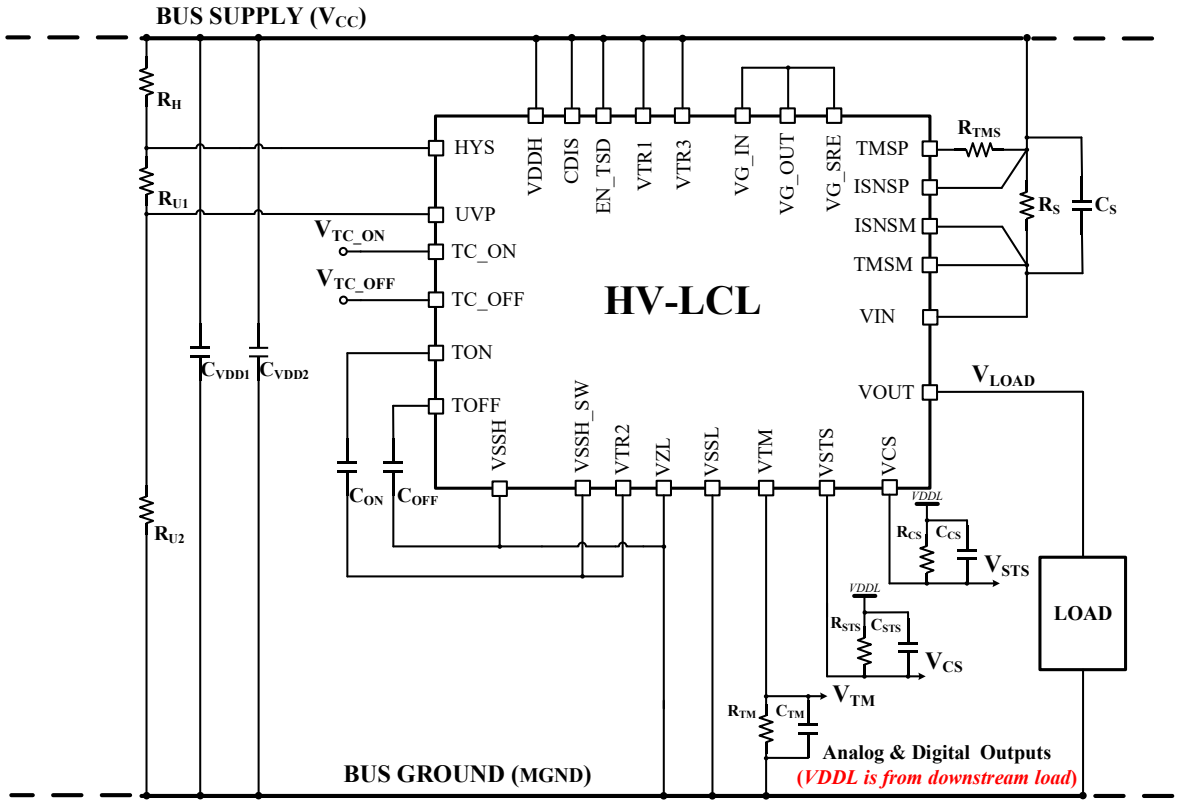
2.1. LCL Configuration (Latch Mode, 5V < V_{CC} ≤ 28V)



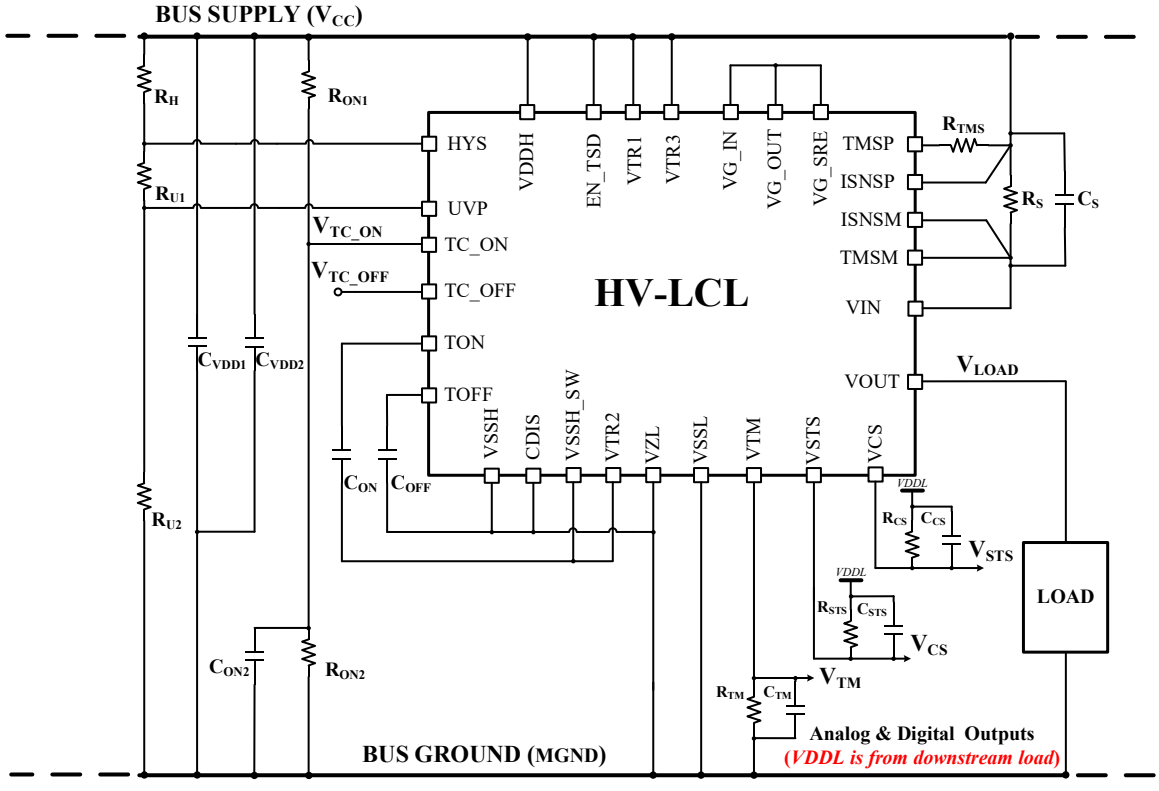
2.2. RLCL Configuration (Re-Triggerable Mode, 5V < V_{CC} ≤ 28V))



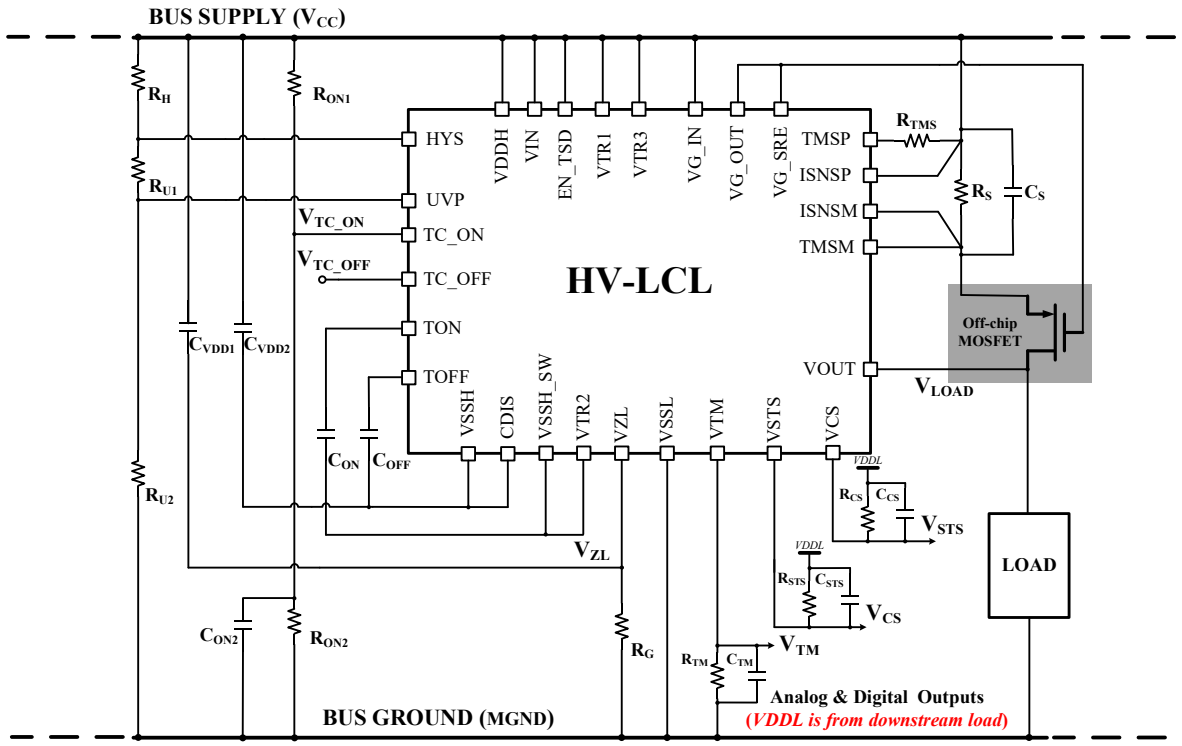
2.3. LCL Configuration (Latch mode, 4V ≤ Vcc ≤ 5V)



2.4. RLCL Configuration (Re-Triggerable mode, 4V ≤ Vcc ≤ 5V)



2.5. RLCL Configuration (Re-Triggerable Mode, with off-chip MOSFET)

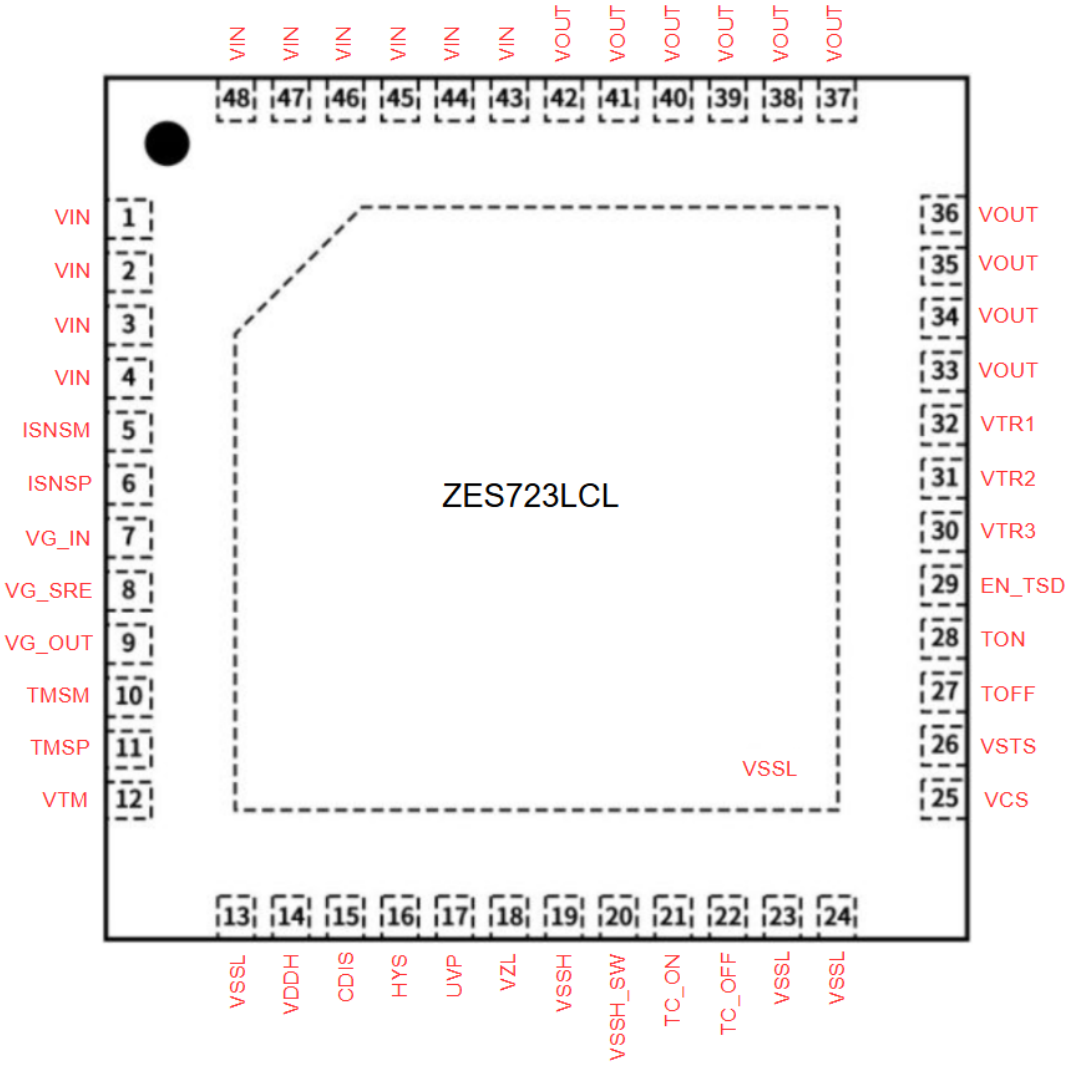


3. Recommended Resistor and Capacitor (RC) Values

Recommended RC Values for LCL (V_{CC} = 28V)				
Symbol	**Class 0.5**	**Class 1**	**Class 2**	**Class 4B**
R_H	1.2KΩ			
R_{U1}	20KΩ			
R_{U2}	220KΩ			
C_{VDD1}	220nF			
C_{VDD2}	220nF			
R_{ON1}	1.1MΩ			
R_{ON2}	100KΩ			
C_{ON2}	1µF			
C_{ON}	1.68µF	1.68µF	1µF	0.356µF
C_{OFF}	10µF (Re-triggerable)/ Short (Latched)			
R_G	10.9KΩ			
R_{TM}	42.2KΩ			
R_{STS}	4.99KΩ			
R_{CS}	4.99KΩ			
C_{TM}	2.2nF			
C_{STS}	2.2nF			
C_{CS}	2.2nF			
R_{TMS}	1KΩ			
R_S	160mΩ	80mΩ	40mΩ	21mΩ
C_S	0.47µF			

4. Pin Configuration

4.1. Preliminary Pin Configurations (QFN48L: 9mm x 9mm Top View)



4.2. Pin Description Table

Table 1. Pin description

Pin	Name	Type	Description
1 to 4, 43 to 48	**VIN**	Power input	Power input of the on-chip power transistor.
5	**ISNSM**	Analog input	Inverting input of the op-amp current limitation loop. The pin is tied directly to the hot (negative) end of the external current sense resistor. Never leave this pin floating.
6	**ISNSP**	Analog input	Non-inverting input of the op-amp current limitation loop. The pin is tied directly to the hot (positive) end of the external current sense resistor. Never leave this pin floating.
7	**VG_IN**	Analog input	Gate of the on-chip power transistor.
8	**VG_SRE**	Analog output	Slew rate enhancement (SRE) for the power transistor.
9	**VG_OUT**	Analog output	Gate drive output for the off-chip power transistor.
10	**TMSM**	Analog input	Inverting input of the telemetry circuit.
11	**TMSP**	Analog input	Non-inverting input of the telemetry circuit.
12	**VTM**	Analog output	Output source current for the analog telemetry. A resistor must be connected between this pin and the true ground.
13, 23, 24, EP	**VSSL**	Power supply	True ground.
14	**VDDH**	Power supply	Supply input voltage.
15	**CDIS**	Digital input	Configuration pin. If connected to VDDH, the embedded counter is disabled.
16	**HYS**	Analog output	External setting of the under-voltage protection block hysteresis. A resistor has to be connected between the supply voltage and this pin.
17	**UVP**	Analog input	External setting of the under-voltage protection block turn-on threshold. The pin must be tied to the mid-point of a resistor divider that senses the supply voltage vs. the true ground.
18	**VZL**	Power supply	Floating ground. Connected to the true ground through a decoupling resistor to operate in the floating ground configuration.
19	**VSSH**	Analog output	Internal circuits dc ground. Zero-voltage reference for all internal circuits.
20	**VSSH_SW**	Analog output	Internal circuits switching ground.
21	**TC_ON**	Digital input	Telecommand interface input for on pulsed signal. Global enable and disable.
22	**TC_OFF**	Digital input	Telecommand interface input for off pulsed signal. Conditional reset and restart.
25	**VCS**	Digital output	Telemetry digital status for the 4-bit counter state. A resistor must be connected between this pin and the ***VDDL**.
26	**VSTS**	Digital output	Telemetry digital status for the tripped state. A resistor must be connected between this pin and the ***VDDL**.
27	**TOFF**	Analog output	Used to set the tripped time. This pin has a double functionality. If the C_{OFF} capacitor is connected between this pin and VSSH, it sets the tripped time value in the RLCL. If the pin is shorted to VSSH, the device is configured in LCL mode.
28	**TON**	Analog output	Used to set the trip-off time. A capacitor C_{ON} is connected between this pin and VSSH_SW.
29	**EN_TSD**	Digital input	Configuration pin. If connected to VDDH, the thermal shutdown (TSD) block is enabled.
30	**VTR3**	Digital input	Trimming code 3 for the sensing voltage (100mV).
31	**VTR2**	Digital input	Trimming code 2 for the sensing voltage (100mV).
32	**VTR1**	Digital input	Trimming code 1 for the sensing voltage (100mV).
33 to 42	**VOUT**	Power output	Power output of the on-chip power transistor.

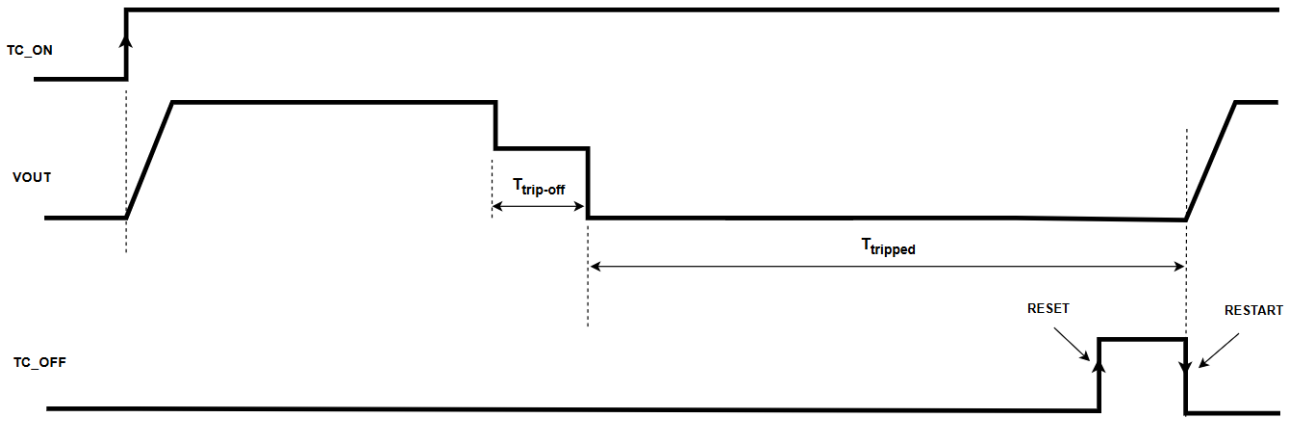
***VDDL** is from downstream load, e.g., FPGA voltage supply.

5. LCL Input Telecommands Scheme (Latch Mode)

TC_ON/TC_OFF	TC_ON = 0	*TC_ON = 1
TC_OFF = 0	OFF	ON
TC_OFF = 1	OFF	When LCL is not tripped, TC_OFF = 1 is blocked. When LCL is tripped, TC_OFF = 1 will reset all internal latches and keeps LCL in **tripped** state and later when switch TC_OFF = 0 will release LCL from trip and turn on VOUT.

**Note: In Latch mode, when TC_ON = 1, set CDS = VDDH (Vcc), otherwise TC_OFF will be blocked.*

5.1. LCL Input Telecommands Timing diagram

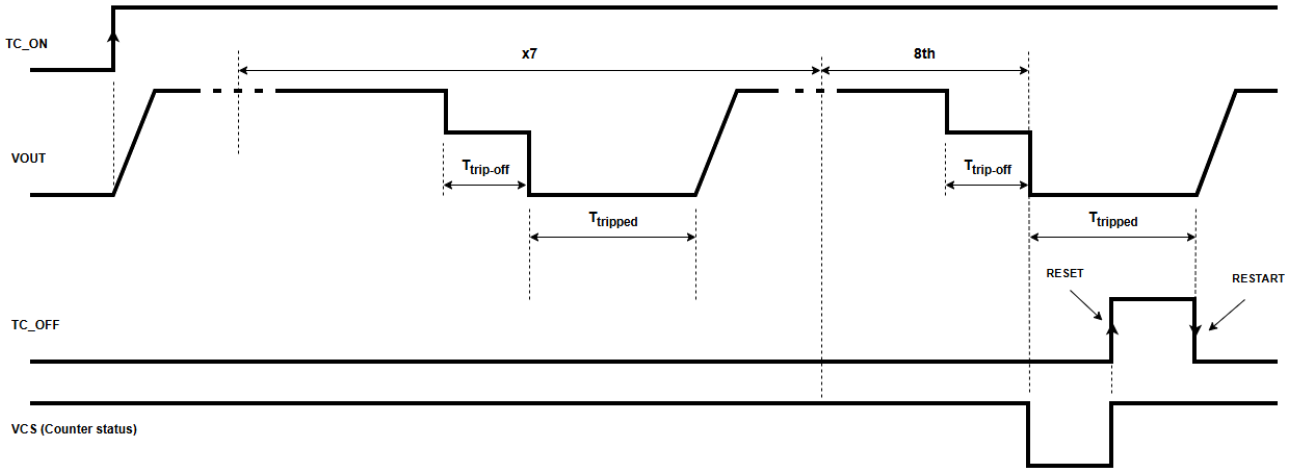


6. RLCL Input Telecommands Scheme (Re-triggerable Mode)

TC_ON/TC_OFF	TC_ON = 0	**TC_ON = 1
TC_OFF = 0	OFF	ON
TC_OFF = 1	OFF	When LCL is **not tripped or Counter counts < 8 times**, TC_OFF = 1 is blocked. When LCL is **tripped and Counter counts ⩾ 8 times**, TC_OFF = 1 will resets all internal latches and keeps LCL in tripped state and stops the retriggering. If later switch TC_OFF = 0 will release LCL from trip and turn on VOUT.

***Note: In Re-Triggerable, when TC_ON=1, set CDS = VSSH (floating ground), otherwise Counter status invalid.*

6.1. RLCL Input Telecommands Timing diagram



7. Specifications and Functions

7.1. Retrigger Functionality

ZES723LCL initiates a Re-trigger Interval when it detects an over-current and the over-current has to last longer than customize **$T_{trip-off}$** time interval.

Re-triggerable LCL (RLCL) retriggering can be stopped (RLCL remains off) by external ground-based command (TC_OFF) if all the two following conditions are true:

- The counter status pin **VCS** goes to low. (The counter status pin **VCS** is clamped to ground when the counter counts 8 times or above of retriggering event, otherwise counter status pin is high.)

- RLCL is in trip state.

7.2. Customizable Settings

ZES723LCL initiates a trip-off Time: 0.5ms – 300ms (minimum trip-off time of 0.5ms to satisfy the HLCL requirements), the **$T_{trip-off}$** can be approximated by the "trip-off" time duration by the following equation.

$$T_{trip-off} \cong T_{ON} \approx 12.6 \times 10^3 \times C_{ON} \quad sec$$

where ***C_{ON}*** is the capacitor connected to **TON** pin.

In typical application, the **$T_{tripped}$** (at Room temp 25degC) can be approximated by the "tripped" time duration by the following equation.

$$T_{tripped} \cong T_{OFF} \approx 2.75 \times 10^6 \times C_{OFF} \quad sec$$

where ***C_{OFF}*** is the capacitor connected to **TOFF** pin.

Limitation (Trip-off) Current that is specified in ECSS-E-ST-20-20C for the following LCL classes: 0.5, 1, 2, 4B.

RLCL classes: 0.5, 1, 2, 4B.

Limitation (Trip-off) Current is defined by R_S with the following equation,

$$I_{limitation\ (Trip-off)} = \frac{100 \times 10^{-3}\ V}{R_S}\ A$$

For operating voltage V_{CC} > 6.6V, the embedded Zener clamp is turned on with the floating ground resistor R_G. R_G is defined with the following equation, where I_{CC} is the total current consumption can be set by user. The recommended value of I_{CC} is 2mA.

$$R_G = \frac{V_{CC} - 6.2}{I_{CC}} \quad \Omega$$

Note: I_{CC} must be greater than 1.5mA.

For operating voltage of 5V < V_{CC} ≤ 6.6V, R_G is set to 200Ω and for operating voltage of 4V ≤ V_{CC} ≤ 5V, just set R_G to zero ohm.

When R_G is fixed, V_{CC} has a lower limit of V_{CC_min}, as shown in the following equation. This equation defines the minimum V_{CC} value that guarantees the normal operation, especially when V_{CC} is unregulated.

$$V_{CC\_min} = R_G * 1.5m + 6.2 \quad V$$

Moreover, the under-voltage lockout (UVLO) turn-on threshold voltage (V_{TH}) should be greater than V_{CC_min}. An under-voltage protection (UVP) circuit protects the device from an incorrect bias condition. The setting of the disconnection and reconnected thresholds (turn-off and turn-on) is performed by means of the R_H-R_{U1}-R_{U2} external divider connected between V_{CC} and MGND. Hysteresis is implemented in order to avoid undesired oscillations caused by bus voltage transients. R_H, R_{U1} and R_{U2} can be chosen using the following equations,

$$V_{TH} = 1.8 \times \frac{R_{U1} + R_{U2}}{R_{U1}} \quad \Omega$$

$$V_{HYS} = V_{TH} - 1.8 \times \frac{R_{U1} + R_{U2} + R_H}{R_{U1} + R_H} \quad \Omega$$

where V_{TH} is the under-voltage lockout turn-on threshold while V_{HYS} is the undervoltage lockout hysteresis.

The telemetry circuit gives information about the current across the load. This circuit provides on the pin VTM a source current whose value is proportional to the current flowing from the bus supply line to the load. V_{TM} is the voltage drop on the external resistor R_{TM}, which reflects the linear conversion of load current (I_{LOAD}) to voltage (V_{TM}).

$$V_{TM} = \frac{R_{TM} \times I_{LOAD} \times R_S}{R_{TMS}} \quad V$$

7.3. Telecommand Interface (3.3V/ 5V)

- **LCL On command** TC_ON pin, level trigger; Active high for both LCL and RLCL; Global enable and disable.

- **LCL Off command/ reset** TC_OFF pin, level trigger; Active high for both LCL and RLCL; Conditional reset and restart (see “Retrigger Functionality”).

7.4. Telemetry Interface

ZES723LCL has an On-Board Telemetry Sensors

Current (5% at Class Current) (Analog Output)

Tripped state status:

When the LCL is off or in the tripped state, VSTS is high as logic “1”; Otherwise, VSTS is low as logic “0”.

Tripped state: If the trip off time criteria is met, the LCL/RLCL is turned off. This off-state of the LCL/RLCL is referred to as tripped state.

Retrigger counter status:

For RLCL, when the retriggering event counter counts 8 times or above, VCS is low as logic “0”; Otherwise, the output voltage is high as logic “1”.

For LCL, the output voltage keeps low as logic “0”.

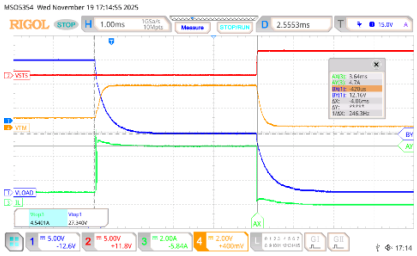
8. Latch, Trip and Re-Triggerable waveform

T_A = 25°C, V_{CC} = 28V, R_G = 10.9kΩ, unless otherwise specified.

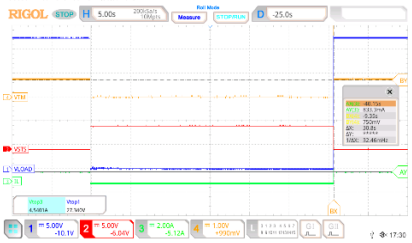
8.1. Class 4B, 28V

Latch

Trip



Re-Triggerable



9. Repetitive Load waveform (Class 4B, 28V)

T_A = 25°C, V_{CC} = 28V, R_G = 10.9kΩ, R_S = 21mΩ, unless otherwise specified.

TBC

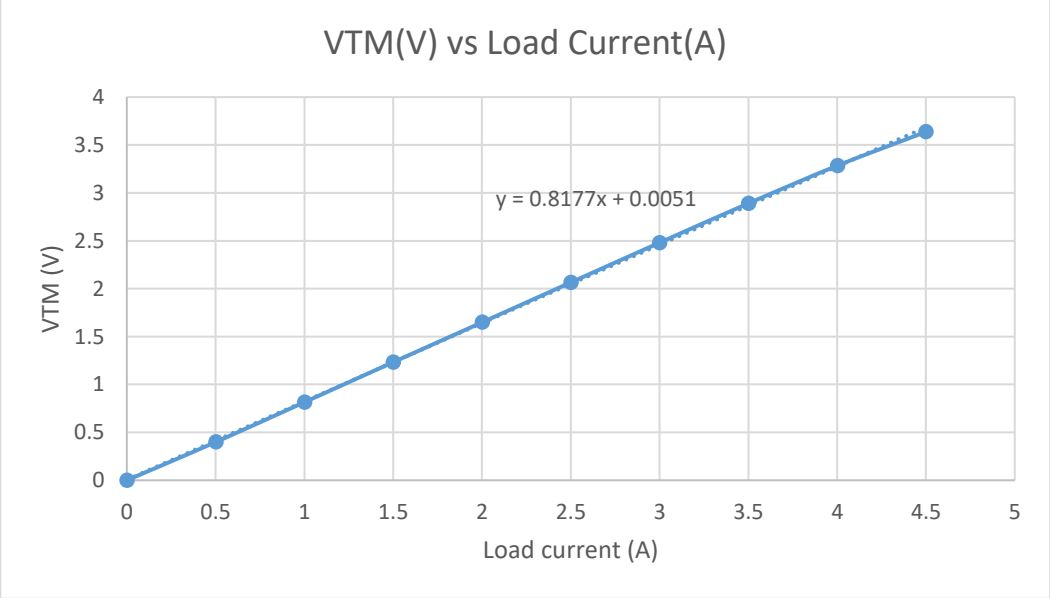
10. Fast transient response (low IL peak) with 300uH loading inductance waveform (Class 4B, 28V)

with Slew Rate Enhancement (SRE) *without Slew Rate Enhancement (SRE)*

TBC

11. VTM vs Load current chart

T_A = 25°C, V_{CC} = 28V, R_G = 10.9kΩ, unless otherwise specified.



12. Electrical characteristics

Table 2. Electrical characteristics

T_A = -40°C to 120°C, V_{CC} = 28V, R_G = 10.9kΩ, R_S = 21mΩ, RLCL configuration, unless otherwise specified.

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	System operating supply voltage		4		28	V
V_Z	Vcc vs. V_{ZL} internal clamp voltage	$V_Z = V_{CC} - V_{ZL}$		5.8	6.2	V
$I_{CC}ON$	Supply current, on-state	V_{CC} = 5V, V_{ZL} = MGND			2	mA
$I_{CC}OFF$	Supply current, off-state	V_{CC} = 5V, V_{ZL} = MGND			200	µA
V_{TH}	Undervoltage lockout turn-on threshold	R_H=1.2kΩ, R_{U1}=20kΩ, R_{U2}=220kΩ		21.6		V
V_{HYS}	Undervoltage lockout hysteresis			1.1		V
V_{LIM}	Current limitation sense voltage threshold			100		mV
R_{DSon}	Power transistor on-resistance				100	mΩ
$V_{gs}ON$	Gate voltage range, on state			4.5		V
$V_{gs}OFF$	Gate voltage range, off state			0		V
T_{ON}	Trip-off time	C_{ON} = 0.356µF (T_{ON} = 12.6K x C_{ON})			4.5	ms
T_{OFF}	Recovery time	C_{OFF} = 10.57µF (T_{OFF} = 2.75M x C_{OFF})		29		s
$T_{DELAY01}$	Delay time (from TC_ON enable to V_{LOAD} = 0 to 10%)	TC_ON and TC_OFF are controlled by telecommands, I_{LOAD} = 1A		0.22		ms
T_{RISE}	Rise time (V_{LOAD} from 10% to 90%)			2.40		
T_{FALL}	Fall time (V_{LOAD} from 10% to 90%)			32.10		
$T_{DELAY02}$	Delay time (from TC_OFF restart to V_{LOAD} = 0 to 10%)			0.22		
V_{TC_ON} V_{TC_OFF}	Telecommand input voltage turn-on/off			1.1		V
T_{pulse}	Telecommand minimum pulse time			68		µs

13. Maximum Ratings

Absolute maximum ratings are limits beyond which damage to the device may occur. Exposure to absolute rating conditions for extended periods may affect device reliability. Functional operation of the device at these conditions is not implied.

Table 3 Absolute maximum ratings

Parameter	Min	Max	Unit
Storage temperature T_{STG}	−55	+150	℃
Operating Junction Temperature T_J		TBC	℃
Thermal resistance junction-case		TBC	℃/W

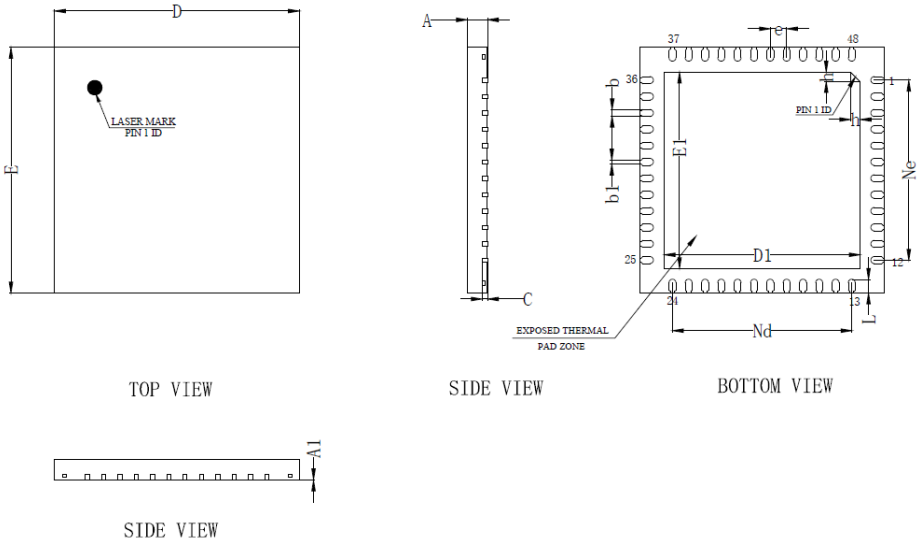
14. ESD Ratings

Table 4 ESD ratings

Parameter	Test Conditions	Value	Unit
ESD Susceptibility	Human Body Model	TBD	V
	Charge Device Model	TBD	V
	Machine Model	TBD	V

15. Package Information

15.1. Package Outline (QFN48L 9mm x 9mm)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.20	0.25	0.30
b1	0.150REF		
c	0.203REF		
D	8.90	9.00	9.10
D1	7.10	7.20	7.30
e	0.60BSC		
Ne	6.60BSC		
Nd	6.60BSC		
E	8.90	9.00	9.10
E1	7.10	7.20	7.30
L	0.45	0.50	0.55
h	0.30	0.35	0.40

16. Soldering Reflow Profiles

Reflow Profiles (per Jedec J-STD-020D.1)	
Profile Feature	**Pb-free Assembly**
Preheat/Soak Temperature Min (Tsmin) Temperature Max (Tsmax) Time (ts) from (Tsmin to Tsmax)	 150˚C 200˚C 60-120 seconds
Ramp-up rate (T_L to Tp)	3˚C/second max.
Liquidous temperature (T_L) Time(tL) maintained above T_L	217˚C 60-150 seconds
Peak package body temperature (Tp)	For users Tp must not exceed the Classification temp in Table 4-2. For suppliers Tp must equal or exceed the Classification temp in Table 4-2.
Time (tp)* within 5˚C of the specified classification temperature (Tc), see Figure 5-1.	30* seconds
Ramp-down rate (Tp to TL)	6˚C/second max.
Time 25˚C to peak temperature	8 minutes max.
* Tolerance for the peak profile temperature (Tp) is defined as a supplier minimum and a user maximum.	

Table 4-2 Pb-Free Process - Classification Temperatures (T_c)

Package Thickness	Volume mm^3 <350	Volume mm^3 350 - 2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm - 2.5 mm	260 °C	250 °C	245 °C
>2.5 mm	250 °C	245 °C	245 °C

Note 1: At the discretion of the device manufacturer, but not the board assembler/user, the maximum peak package body temperature (T_p) can exceed the values specified in Tables 4-1 or 4-2. The use of a higher T_p does not change the classification temperature (T_c).

Note 2: Package volume excludes external terminals (e.g., balls, bumps, lands, leads) and/or nonintegral heat sinks.

Note 3: The maximum component temperature reached during reflow depends on package thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD packages may still exist.

Note 4: Moisture sensitivity levels of components intended for use in a Pb-free assembly process **shall** be evaluated using the Pb-free classification temperatures and profiles defined in Tables 4.2 and 5-2, whether or not Pb-free.

Note 5: SMD packages classified to a given moisture sensitivity level by using Procedures or Criteria defined within any previous version of J-STD-020, JESD22-A112 (rescinded), IPC-SM-786 (rescinded) do not need to be reclassified to the current revision unless a change in classification level or a higher peak classification temperature is desired.

Table 5-1 Moisture Sensitivity Levels

LEVEL	FLOOR LIFE		SOAK REQUIREMENTS				
			STANDARD		ACCELERATED EQUIVALENT[1]		
					eV 0.40-0.48	eV 0.30-0.39	
	TIME	CONDITION	TIME (hours)	CONDITION	TIME (hours)	TIME (hours)	CONDITION
1	Unlimited	≤30 °C/85% RH	168 +5/-0	85 °C/85% RH	NA	NA	NA
2	1 year	≤30 °C/60% RH	168 +5/-0	85 °C/60% RH	NA	NA	NA
2a	4 weeks	≤30 °C/60% RH	696[2] +5/-0	30 °C/60% RH	120 +1/-0	168 +1/-0	60 °C/60% RH
3	168 hours	≤30 °C/60% RH	192[2] +5/-0	30 °C/60% RH	40 +1/-0	52 +1/-0	60 °C/60% RH
4	72 hours	≤30 °C/60% RH	96[2] +2/-0	30 °C/60% RH	20 +0.5/-0	24 +0.5/-0	60 °C/60% RH
5	48 hours	≤30 °C/60% RH	72[2] +2/-0	30 °C/60% RH	15 +0.5/-0	20 +0.5/-0	60 °C/60% RH
5a	24 hours	≤30 °C/60% RH	48[2] +2/-0	30 °C/60% RH	10 +0.5/-0	13 +0.5/-0	60 °C/60% RH
6	Time on Label (TOL)	≤30 °C/60% RH	TOL	30 °C/60% RH	NA	NA	NA

Note 1: CAUTION - To use the "accelerated equivalent" soak conditions, correlation of damage response (including electrical, after soak and reflow), should be established with the "standard" soak conditions. Alternatively, if the known activation energy for moisture diffusion of the package materials is in the range of 0.40 - 0.48 eV or 0.30 - 0.39 eV, the "accelerated equivalent" may be used. Accelerated soak times may vary due to material properties (e.g., mold compound, encapsulant, etc.). JEDEC document JESD22-A120 provides a method for determining the diffusion coefficient.

Note 2: The standard soak time includes a default value of 24 hours for semiconductor manufacturer's exposure time (MET) between bake and bag and includes the maximum time allowed out of the bag at the distributor's facility.

If the actual MET is less than 24 hours the soak time may be reduced. For soak conditions of 30 °C/60% RH, the soak time is reduced by 1 hour for each hour the MET is less than 24 hours. For soak conditions of 60 °C/60% RH, the soak time is reduced by 1 hour for each 5 hours the MET is less than 24 hours.

If the actual MET is greater than 24 hours the soak time must be increased. If soak conditions are 30 °C/60% RH, the soak time is increased 1 hour for each hour that the actual MET exceeds 24 hours. If soak conditions are 60 °C/60% RH, the soak time is increased 1 hour for each 5 hours that the actual MET exceeds 24 hours.

Note 3: Supplier may extend the soak times at their own risk.

17. Revision History

Version No.	Notes	Date
V0.0.1	Preliminary version	27th Nov. 2025
V0.0.2	Included TID test result	26th Feb. 2026

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