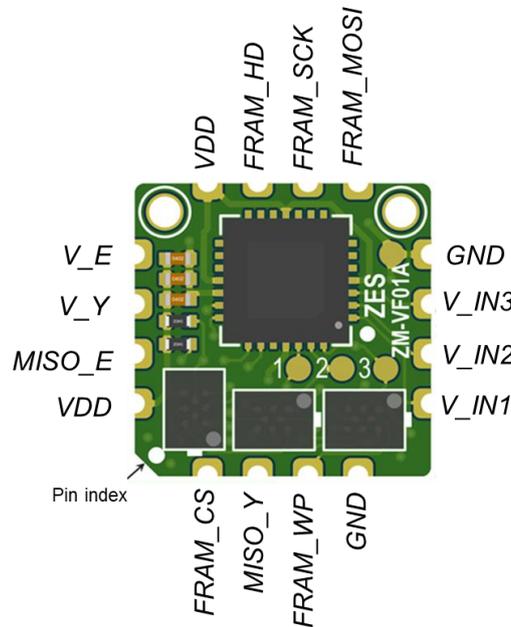


# Radiation-Hardened Triple-Modular-Redundancy FRAM + Voter Channel (ZM-VF01A)

Enabling Advanced Commercial-Off-The-Shelf (COTS) to 'Space-Grade'



## Overview

ZM-VF01A is a radiation-hardened Triple-Modular-Redundancy (TMR) Ferroelectric Random Access Memory (FRAM) module embodying a ZES400 (or ZES401) voter and three 1M-bit FRAMs implemented in TMR. The ZES400/ZES401 voter embodies 4-channel voting circuits where one of the channels is used to vote the outputs of the FRAMs. An additional voter channel is available for supporting TMR for another signal where necessary. The ZM-VF01A features ultra-low error, suitable for storing critical data storage and/or supporting ZES error-detection-and-correction (ZEDAC) algorithms.

## Key Features

- Radiation-hardened ZES400/401 voter adopted (Total Ionizing Dose @ 300krad (Si), Single-Event-Latchup (SEL) @ 110MeV-cm<sup>2</sup>/mg and Single-Event-Upset (SEU) @ 83MeV-cm<sup>2</sup>/mg)

- FRAM with inherent SEU radiation hardness
- Operating voltage: 1.8V – 3.6V
- Temperature: -40°C to 85°C
- SPI interface with the FRAMs
- Additional voter channel available for enabling TMR for another customized signal
- **Overall TID: 45krad (Si)**
- **Laser test on FRAMs – no SEL @ up to 5.5nJ laser energy**
- **Overall proton test: no SEU/SEL up to 200MeV**

## Applications

- Low power embedded applications for CubeSat payloads for Low-Earth-Orbit (LEO)
- Telemetry/data communication applications
- Low error-rate data protection applications
- Instrumentation and control for high reliability applications
- Support ZEDAC algorithms for data integrity protection on memories

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## 1 Overview

ZM-VF01A is a radiation-hardened Triple-Modular-Redundancy (TMR) Ferroelectric Random Access Memory (FRAM) module embodying a ZES400 (or ZES401) voter and three 1M-bit FRAMs implemented in TMR. The ZES400/ZES401 voter embodies 4-channel voting circuits where one of the channels is used to vote the outputs of the FRAMs. An additional voter channel is available for supporting TMR for another signal where necessary. The ZM-VF01A features ultra-low error, suitable for storing critical data storage and/or supporting ZES error-detection-and-correction (ZEDAC) algorithms.

### 1.1 Features

- Radiation-hardened ZES400/401 voter adopted (Total Ionizing Dose @ 300krad (Si), Single-Event-Latchup (SEL) @ 110MeV-cm<sup>2</sup>/mg and Single-Event-Upset (SEU) @ 83MeV-cm<sup>2</sup>/mg)
- FRAM (part number: MB85RS1MT) with inherent SEU radiation hardness
- Operating voltage: 1.8V – 3.6V
- Temperature: -40°C to 85°C
- SPI interface with the FRAMs
- Additional voter channel available for enabling TMR for another customized signal
- **Overall Total Ionizing Dose (TID): 45krad (Si)**
- **Laser test on FRAMs – no Single-Event-Latchup (SEL) @ up to 5.5nJ laser energy**
- **Overall proton test: no SEU/SEL up to 200MeV**

### 1.2 Block Diagram

Fig. 1 depicts the simplified diagram of ZM-VF01A, showing various ZES400/401 and FRAM components and their interface signals/connections. The primary inputs/outputs are shown; their pin definitions are delineated in Table 1 of Section 2.1.

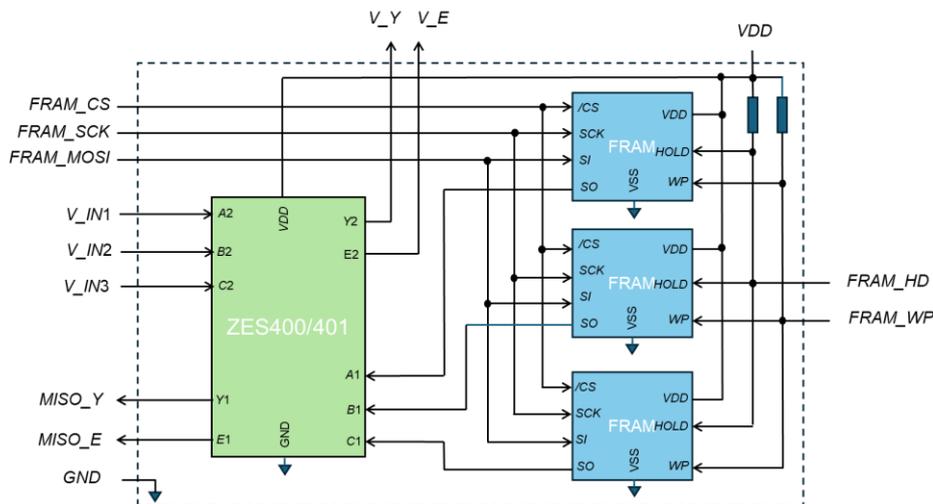


Fig. 1: The simplified block diagram of ZM-VF01A

### 1.3 Ordering Information

#### Ordering Information

PART No.	Size
ZM-VF01A	11.8 mm x 11.8 mm
ZEDAC	Software

For further price, delivery, and ordering information please contact [info@zero-errorsystems.com](mailto:info@zero-errorsystems.com).

## 2 Signal/Pins and Operation Control

Fig. 2 depicts the pin assignment of ZM-VF01A.

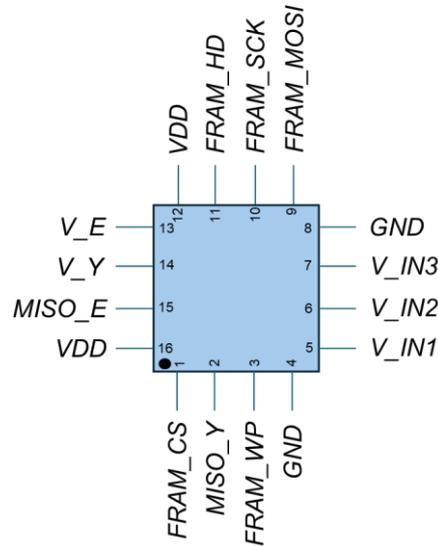


Fig. 2: Pin assignment of ZM-VF01A

### 2.1 Module Input/Output (I/O)

Table 1: I/O Signals

S/N	Pin Name	I/O Type	Pin Description	Remark
1	<i>FRAM_CS</i>	Input	FRAM Chip Select pin	See Figs. 1 and 2 for the locations
2	<i>MISO_Y</i>	Output	FRAM Serial Data Output pin (through ZES400/401)	
3	<i>FRAM_WP</i>	Input	FRAM Write Protect pin (with a pull-up resistor onboard)	
4	<i>GND</i>	Ground	Ground pin	
5	<i>V_IN1</i>	Input	ZES400/401 Voter Channel Input 1 pin	
6	<i>V_IN2</i>	Input	ZES400/401 Voter Channel Input 2 pin	
7	<i>V_IN3</i>	Input	ZES400/401 Voter Channel Input 3 pin	
8	<i>GND</i>	Ground	Ground pin	
9	<i>FRAM_MOSI</i>	Input	FRAM Serial Data Input pin	
10	<i>FRAM_SCK</i>	Input	FRAM Serial Clock pin	
11	<i>FRAM_HD</i>	Input	FRAM Hold pin (with a pull-up resistor onboard)	
12	<i>VDD</i>	Power	Supply Voltage pin	
13	<i>V_E</i>	Output	ZES400/401 Voter Channel Output for Error pin	
14	<i>V_Y</i>	Output	ZES400/401 Voter Channel Voted Data Output pin	
15	<i>MISO_E</i>	Output	FRAM Serial Data Output Error pin (through ZES400/401)	
16	<i>VDD</i>	Power	Supply Voltage pin	

### 2.2 FRAM SPI Operation Control

Fig. 3 depicts the SPI control modes for accessing the FRAMs. Please note that for each operation (e.g., write or read), the three FRAMs are written/read simultaneously.

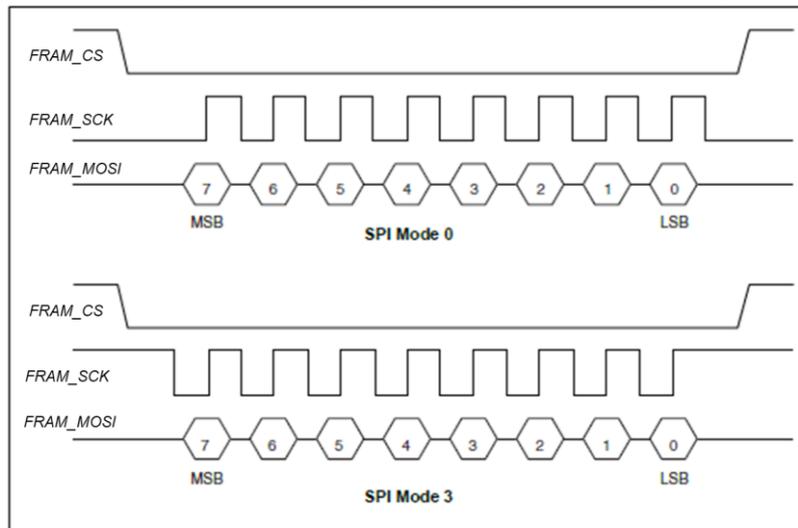
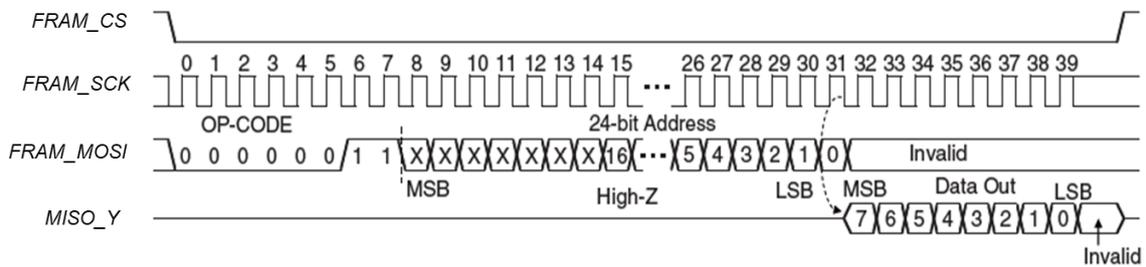


Fig. 3: The SPI modes for accessing FRAMs

### 2.3 FRAM Access Timing Diagram

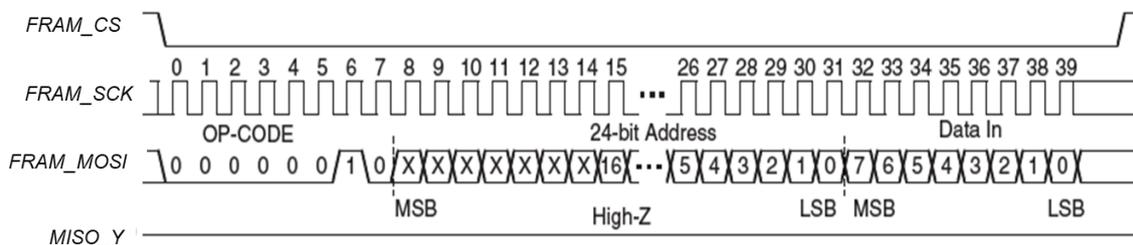
Figs. 4 (a) and (b) depict the access timing diagrams for the read operation and write operation, respectively.

#### READ Operation



(a)

#### WRITE Operation



(b)

Fig. 4: The access timing diagram: (a) read operation, and (b) write operation

### 2.4 Voter Channel Control

Table 2 tabulates the truth table of the voter channel.

Table 2: Voter Channel Truth Table

V_IN1	V_IN2	V_IN3	V_Y	V_E
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	1
1	0	0	0	1
1	0	1	1	1
1	1	0	1	1
1	1	1	1	0

## 3 Technical Specifications

### 3.1 Recommending Conditions

Table 3 tabulates the recommended conditions for operating ZM-VF01A.

Table 3: Recommended Conditions

Symbol	Parameter	Min	Typ	Max	Unit	
$T$	Temperature range	-40	-	+85	°C	
$V_{DD}$	Voltage supply of the module	1.8	3.3	3.6	V	
$V_i$	Input voltage	0	-	$V_{DD}$	V	
$V_o$	Output voltage	0	-	$V_{DD}$	V	
$f$	Maximum frequency (RT*, 3.3V, 4.75pF*)	-	-	20	MHz	
$I_{CC}$	Max. Power Typ. @ RT*, 3.3V, 20MHz FRAM Read/Write, 4.75pF* Max. @ 85°C, 3.6V, 20MHz FRAM Read/Write, 4.75pF*	-	TBD	TBD	mA	
$V_{IH}$	High-level input voltage	$V_{DD}=1.8\pm 10\% V$	1.26	-	-	V
		$V_{DD}=3.3\pm 10\% V$	2.32	-	-	V
$V_{IL}$	Low-level input voltage	$V_{DD}=1.8\pm 10\% V$	-	-	0.54	V
		$V_{DD}=3.3\pm 10\% V$	-	-	0.99	V
$I_{OH}$	High-level output current	$V_{DD}=1.8\pm 10\% V$	-	-	-2	mA
		$V_{DD}=3.3\pm 10\% V$	-	-	-4	mA
$I_{OL}$	Low-level output current	$V_{DD}=1.8\pm 10\% V$	-	-	2	mA
		$V_{DD}=3.3\pm 10\% V$	-	-	4	mA
$t_r, t_f$	Input rise or fall time (10% to 90%)	$V_{DD}=1.8\pm 10\% V$	-	-	1000	ns
		$V_{DD}=3.3\pm 10\% V$	-	-	400	ns

\*Assuming capacitance due to PCB traces is negligible

\*RT: Room Temperature

### 3.2 Reliability Tests

The following test results are summarized below in Table 4. For detailed test results, please contact [info@zero-errorsystems.com](mailto:info@zero-errorsystems.com)

Table 4: Reliability Tests

Parameter	Condition	Value*	Units
Proton Testing	Proton fluence = TBD; no SEL/SEU	200	MeV
Total Ionizing Dose	Cobalt-60 @ Kyushu University	45k	rad
SEL @ Laser	Laser Testing on FRAMs; no SEL	5500	pJ

\* The value was the characterized value during the test was observed.

### 3.3 Physical Dimensions

Fig. 5 depicts the physical outline dimension for ZM-VF01A. Fig. 6 depicts the recommended footprint while integrating ZM-VF01A into another module.

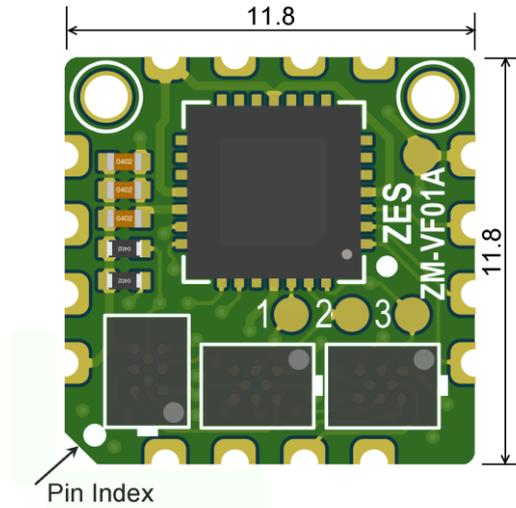


Fig. 5: Physical outline dimension

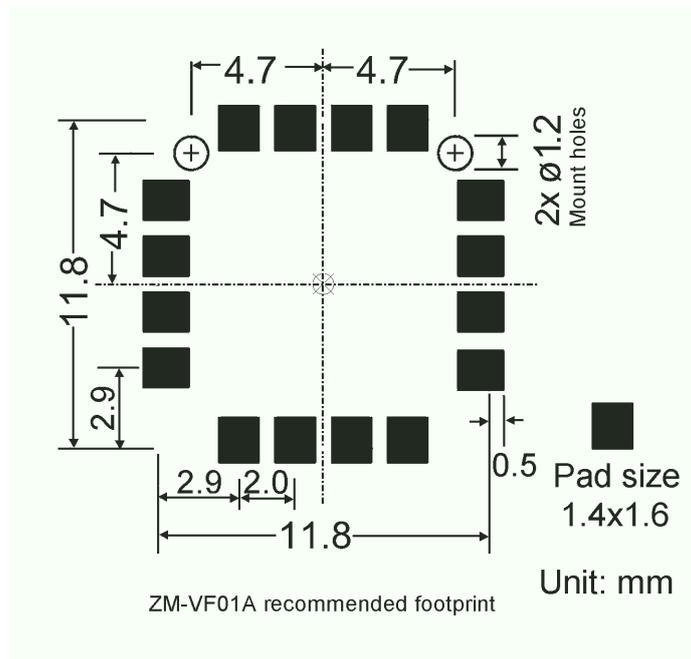


Fig. 6: Recommended footprint

## 4 Recommended Interface

Fig. 7 depicts the recommended interface connection when a microcontroller or a Field-Programmable-Gate-Array (FPGA) is connected to ZM-VF01A via an SPI interface. Please note that the pull-up resistor R1 and the pull-down resistor R2 could be optional if the microcontroller or the FPGA can provide sufficient current drive to drive ZM-VF01A. If not, please refer back to the datasheet of the microcontroller or the FPGA to provide appropriate R1 and/or R2 values to drive ZM-VF01A.

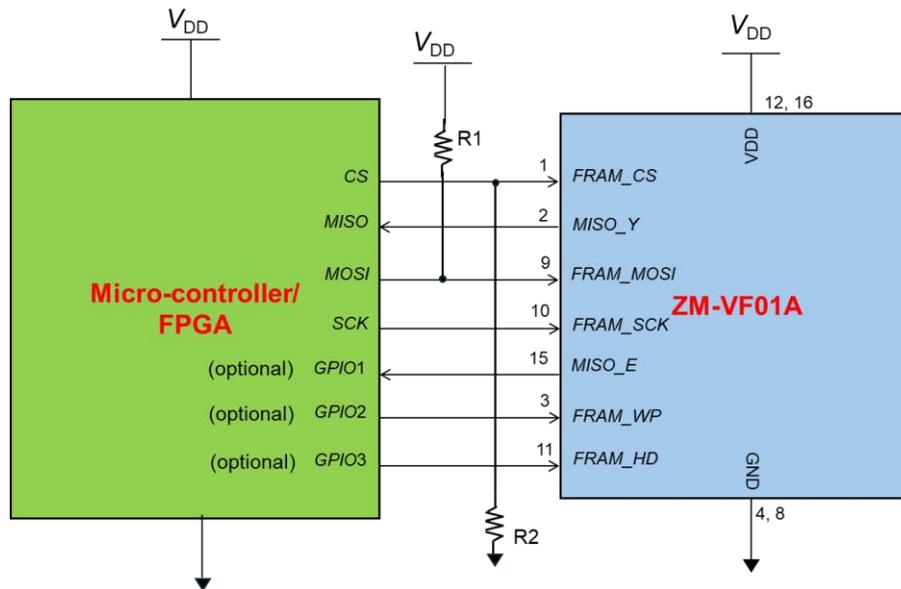


Fig. 7: Recommended interface connection between a microcontroller/FPGA and ZM-VF01A. The pull-up resistor R1 and pull-down resistor R2 could be optional.

## 5 Application Examples

### 5.1 Hardware/software co-solution for enabling ZES Error Detection-and-Correction (ZEDAC) algorithm

ZM-VF01A can be integrated with the ZES error-detection-and-correction (ZEDAC) algorithm(s) to enable data protection virtually for any memories (e.g., eMMC or DDR4). Fig. 8 briefly depicts the interface setup where a processing unit embodying either a microcontroller (MCU) or an FPGA. The processing unit is interfaced with an external memory and ZM-VF01A. The external memory could be a Commercially-Off-the-Shelf (COTS) memory (e.g., eMMC or DDR4) whose data need to be protected. The ZEDAC algorithm is executed within the MCU/FPGA, providing the encoding/decoding process. The ZM-VF01A and the ZEDAC algorithm collectively serve as a hardware/software co-solution to reduce the soft-error (e.g., bit flips) in the external memory. The hardware/software co-solution provides 50x better error-rate than the hardware-only solution, and 2000x better error-rate than the solution-only solution. For more information about ZEDAC, please contact [info@zero-errorsystems.com](mailto:info@zero-errorsystems.com).

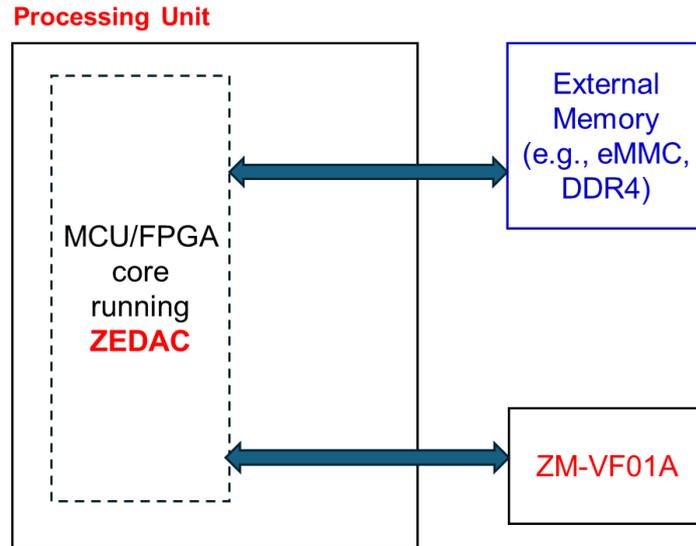


Fig. 8: Setup for enabling hardware/software co-solution to feature ultra low soft-error rate (in part using ZM-VF01A and ZEDAC)

## 5.2 Add-on Connector for Interfacing a System with SPI Ports

ZM-VF01A can be mounted to a customized add-on connector which can be interfaced with a system/subsystem via the GPIO pins. Fig. 9 depicts an example where the add-on connector is designed to embody the ZM-VF01 module, and to have a 40-pin interface compatible with a Nvidia Nano Orin system. With the add-on connector, the ZM-VF01 is inherently connected (via the SPI ports) to the MCU of the Nvidia Nano Orin system. If necessary, the ZEDAC algorithm can be easily executed in the MCU, checking/recovering the data using the MCU and the ZM-VF01. The data could be embedded SRAMs within the MCU, or the dedicated eMMC/DDR memories within the Nvidia Nano Orin system.

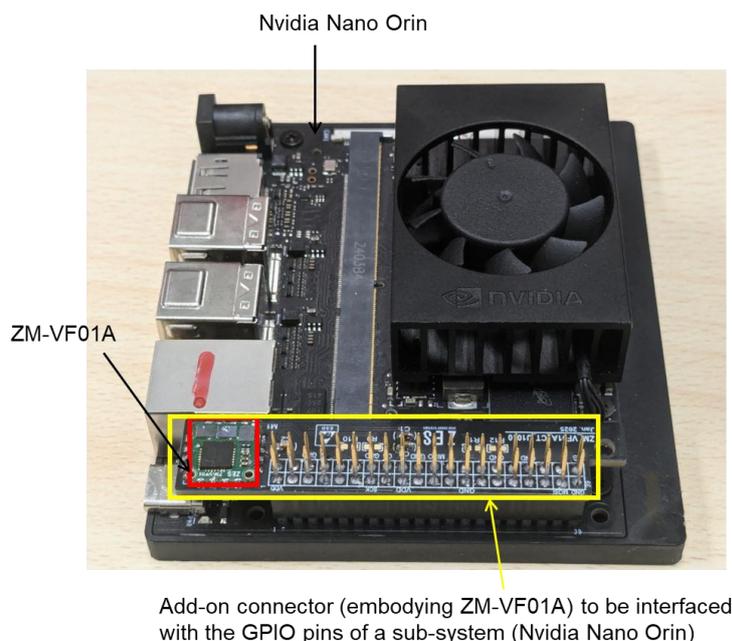


Fig. 9: An example – ZM-VF10A on a connector which is interfaced with a Nvidia Nano Orin module (via its 40-pin GPIOs)

Similarly, the add-on connector can be customized for other systems/subsystems such as Raspberry Pie systems/sub-systems. For more information about the add-on connector, please contact [info@zero-errorsystems.com](mailto:info@zero-errorsystems.com).

### 5.3 Critical data storage

ZM-VF01A can be used to store critical data such as the boot programs, critical configuration data, AI-model data, critical output data, and critical operational status information for satellite applications or high reliability applications. Please note the memory capacity limit is 1M-bit.

### 5.4 Voter Channel Application

ZM-VF01A has an additional voting channel which can enable TMR for two sub-systems. Fig. 10 depicts an example how the data can be transferred, via ZM-VF01A, between the two sub-systems A and B. In the sub-system A, three sub-circuits T1, T2 and T3 generate three same signals  $T_a$ ,  $T_b$ , and  $T_c$  which are voted by ZM-VF01A to generate a voted output  $T_y$ . The three sub-circuits T1, T2 and T3 are usually the same. The voted output  $T_y$  is virtually SET-hardened. The voter output  $T_y$  is virtually error-free provided that the error possibility to have two erroneous signals (out of the three signals  $T_a$ ,  $T_b$ , and  $T_c$ ) is assumed to be very low. The error indication signal  $T_e$  can be used to alert the sub-system B, indicating that at least one of the three signals  $T_a$ ,  $T_b$ , and  $T_c$  is different.

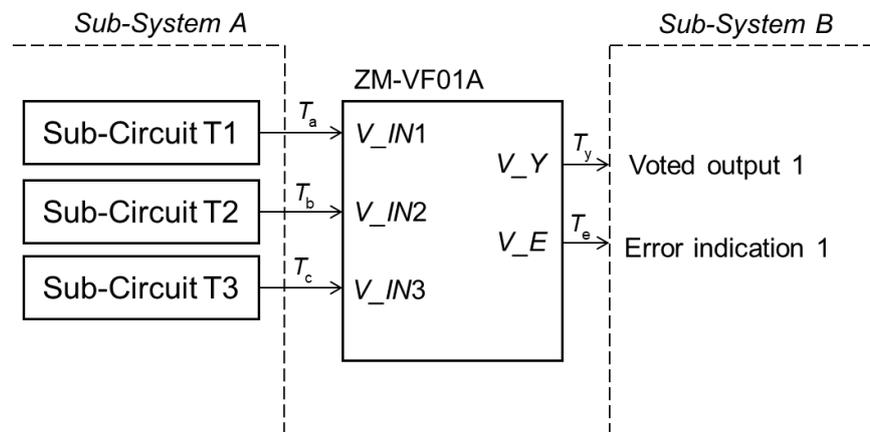


Fig. 10: TMR application example using the voter channel

## 6 Revision History

Version	Description	Date
V1.0	First version	Mar-2025
V1.1	Diagram updated, TID result included	May-2025

For the latest version of this document, please contact us [info@zero-errorsystems.com](mailto:info@zero-errorsystems.com).

## 7 Legal

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