ZERO-ERROR SYSTEMS

ZES100 (LDAP-IC)

Rev 3.5/ Nov 2025

ZES100- Latchup Detection and Protection (LDAP) Application Note

Abstract

The Application Note delineates the unique features and advantages of ZES100 Latchup Detection And Protection (LDAP) IC, compared with conventional Latchup Current Limiter (LCL). In short, LDAP is designed to protect non-rad-hard semiconductor COTS (Commercial-off-the-Shelf) components from radiation effects, particularly Single-Event-Latchup (SEL) and/or micro-SEL (μ-SEL).

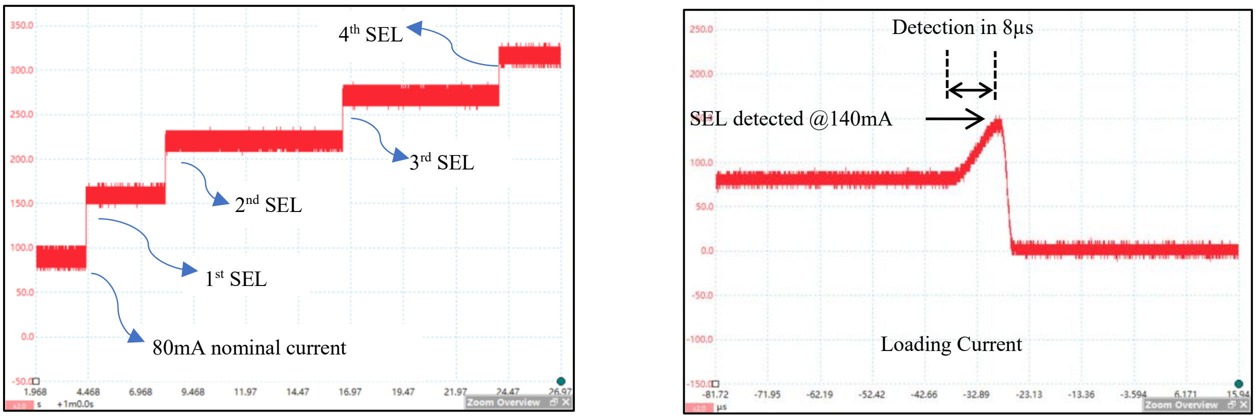
Contents

1. Introduction

ZES100 LDAP-IC is a radiation-hardened monolithic microchip, dedicatedly designed for space/satellite applications, protecting non-radiation-hardened microchips from radiations, particularly Single-Event-Latchup (SEL) and/or micro-SEL (µSEL).

SEL is commonly observed as a phenomenon akin to a short-circuit current. On the other hand, µSEL is not well reported as its current surge is often relatively small, hence mostly unnoticeable. As microchips are getting more advanced and sophisticated, µ-SEL therein is more prevalent.

Figure 1 (a) depicts a waveform of an accumulated µSEL current from a Commercial-Off-The-Shelf (COTS) FPGA induced by a laser. Multiple µSEL events are observed and every µSEL event only incurs a very small increase of current. If a conventional current limiter is implemented to protect this FPGA, the conventional current limiter would miss the first few µSEL events, hence highly compromising the reliability of the FPGA. Note that the occurrence of these multiple µSEL events is accelerated during the laser tests. In the actual space environment, the occurrence of the µSEL event is totally random, and the time interval between two µSEL events can be weeks or even months.



(a) (b)

Figure 1 (a) Demonstrations of accumulated µSELs induced by Laser, (b) Detection of µSEL by LDAP

ZES LDAP is designed to detect both SEL and µSEL based ZES' proprietary technology. Specifically, ZES LDAP continuously monitors and analyzes the loading current, and is able to intelligently detect the transient profile of SEL and/or µSEL current, and subsequently performs a power-cycling to protect the FPGA.

**ZES LDAP itself is radiation hardened, immune to any Single-Event Effects including Single-Event Latchup (SEL), Single-Event Transient (SET), Single-Event Upset (SEU), etc. of >110MeV-cm^2/mg, and to Total Ionized Dose (TID) of >300Krad.

2. ZES100 LDAP Solution

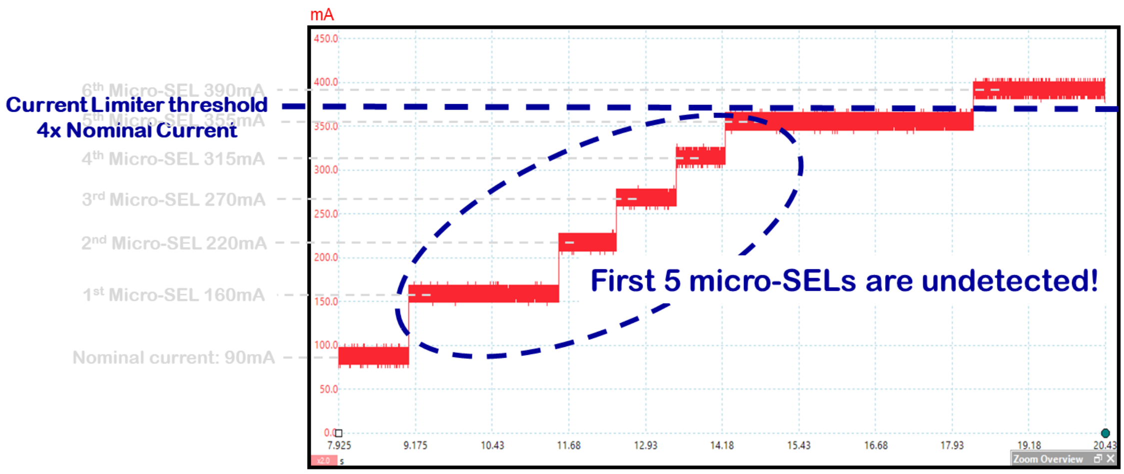
ZES100, embodying ZES' proprietary Latchup detection patented technology, offers unprecedented advantages over the conventional Latchup Current Limiter (LCL).
Specifically, ZES LDAP offers:

(a) **First level of protection for micro-SEL (µSEL) with quick detection.**
(b) **Second level of protection of major-SEL and other current anomalies.**
(c) **Immunity to false triggers; and**
(d) **Radiation hardened, Space qualified high reliability semiconductor.**

Each feature will now be delineated in turn.

First, the **features in (a) and (b)** are delineated together as they address a similar problem, SEL, which is well recognized as the top concern for CMOS-based COTS ICs/SoCs in a radiation environment.

The mechanism of SEL has been well established, and consequently, the SEL has been conventionally treated as a general over-current event – we call it major-SEL. However, as COTS ICs/SoCs become advanced and sophisticated, the SEL behavior of these ICs/SoCs also turns to be more complex. Specifically, the SEL events of many advanced COTS ICs/SoCs do not resemble the general over-current events whose current mostly surges to a very high level. Conversely, these SEL events are often localized within a small silicon region, hence exhibiting a low SEL current – we call it micro-SEL (µSEL).
Figure 2 depicts several µSEL events in a commercial grade COTS FPGA, induced by an accelerated laser test, whose µSEL current is very small, comparable with the nominal operating current. There are two distinctions between major-SEL and µSEL. First, major-SEL often inflicts a rapid damage to ICs as the induced major-SEL current is mostly high, while µSEL typically does a postponed damage as the induced µSEL current is mostly low. Second, the rapid damage by major-SEL often exhibits as burning, while the postponed damage by µSEL often exhibits as electromigration. Further note that, in a practical radiation environment, the SEL events are totally random, and hence the interval between two µSEL can be in weeks or even months, unlike that in **Figure 2** as it is the results of an accelerated test.



Y He, *et al.*, J Chang, RADECS Conf, Oct 2022

Figure 2 µSEL current in a COTS FPGA

At this juncture, the common practice for SEL protections in satellites is a conventional Latching Current Limiter (LCL). The LCL has been effective in the past as most of the SEL events in traditional CMOS-based COTS ICs are major-SEL. However, it is increasingly challenging to protect µSEL by the conventional LCL. Taking the example in **Figure 2**, wherein the nominal current is 90mA, and the CL threshold is typically set at 360mA, 4X of the nominal current, it can be observed that the conventional LCL would miss the first 5 µSEL events, the elevated SEL current would gradually damage the COTS FPGA due to electromigration, hence highly compromising the reliability of the COTS FPGA.

It is even harder to implement the conventional LCL to protect a complex COTS computation system. **Figure 3(a)** illustrates an example of the operation of the complex computation system that embodies a low-computation mode at a low operating current of 20mA and a high-computation mode at a high operating current of 230mA. When μSEL occurs, the total current including the μSEL current jumps to 150mA. In this example, designers would find it extremely difficult to set the current limit threshold when the conventional LCL is employed. Specifically, if the current limit threshold is set low according to the low operating current as depicted in **Figure 3(b)**, μSEL can be detected, but the high-computation mode would incur a false trigger to LCL. On the other hand, if the current limit threshold is set high according to the high operating current as depicted in **Figure 3(c)**, μSEL would be detected.

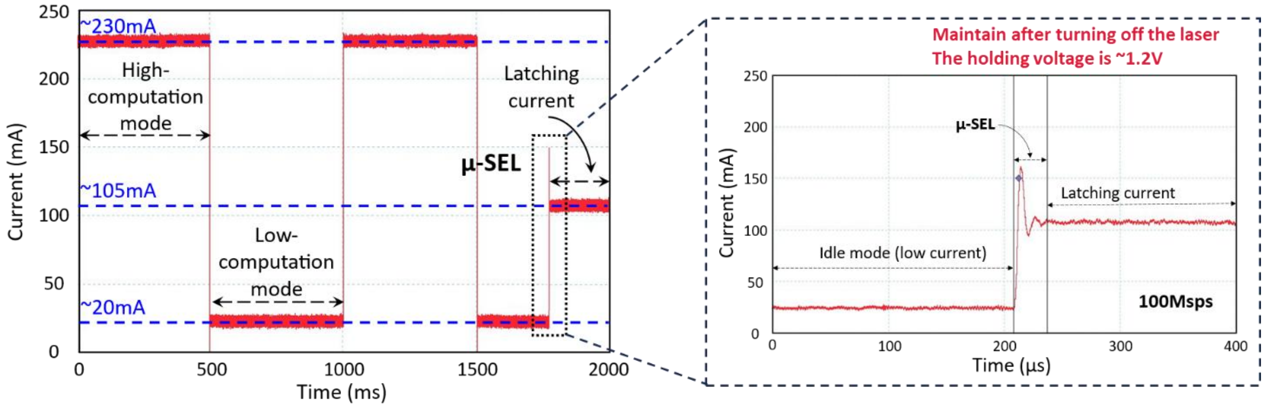


Figure 3(a)

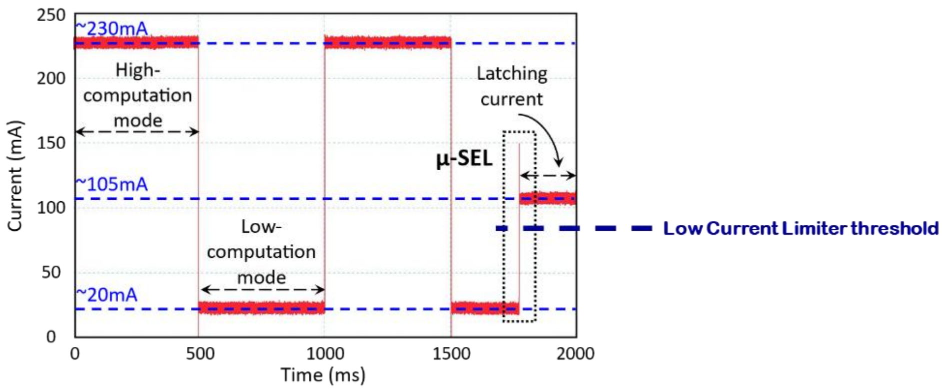


Figure 3(b)

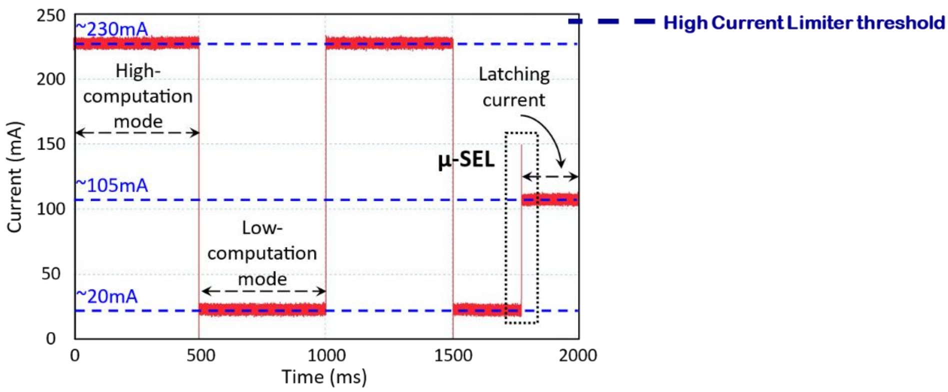


Figure 3(c)

Figure 3 A complex COTS computation system embodying low and high computation currents: (a) μSEL, (b) protected by a low CL threshold, (c) not protected by a high CL threshold

In short, the conventional LCL is unable to protect advanced and complex ICs/SoCs from SEL, in particular µSEL.

ZES LDAP embodies two levels of protection. The first level of protection is to detect µSEL by a proprietary SEL current detector, which intelligently detects µSEL by analyzing and distinguishing the transient µSEL current profile.
Figure 4 depicts the waveforms of the µSEL current when being detected and subsequently protected by ZES LDAP. It can be observed that the µSEL detection only takes 8µs, and the µSEL only increases by 60mA (=140mA-80mA).

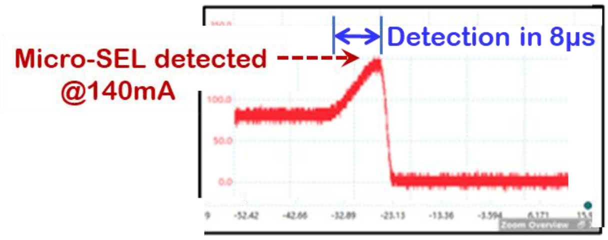


Figure 4 µSEL detection and protection by ZES LDAP

The second level of protection serves to complement the first level of protection by detecting major-SEL and other current anomalies. The second protection is akin to the conventional LCL, wherein a current threshold is implemented. However, as a complementary level of protection, it typically embodies a current threshold far away from the operating current, hence only being triggered when a destructively high current appears; note that this scenario is largely rare in real applications.

In short, ZES LDAP provides unprecedented detection and protection for µSEL, major-SEL and other current anomalies.

Second for **feature (c)**, ZES LDAP is advantageous over the conventional LCL as it is designed to be immune to false triggers. Three scenarios may introduce false triggers. The first is an operating current swing between a low-computation mode and a high-computation mode.
As mentioned above for **Figures 3(b) and 3(c),** the false trigger happens when the current threshold of the conventional LCL is low, but setting the current threshold high to avoid the false trigger may incur protection failures. ZES LDAP doesn't exhibit any false triggers in this case. Specifically, its first level of protection is innately immune to this scenario, as ZES LDAP is designed to only detect the unique transient profile of the SEL current, which is very distinct from the transient current swinging from low to high. Further, its second level of protection, as the complementary protection, can be set higher than the current at the high-computation mode.
The second is a transient operating current spike. The current spike is typically large and fast and may temporarily exceed the current threshold of the conventional LCL, hence triggering the protection falsely. A blank time is often implemented to avoid this, and ZES LDAP is also immune to this phenomenon. Specifically, akin to the first, its first level of protection can intelligently distinguish the transient SEL current from the transient current spike, and its second level of protection is also insensitive to it as a similar blank time is realized therein.
The third is a gradual operating current increase over an operational lifetime, and this current increase is largely induced by radiation. As the current threshold of the conventional LCL is mostly fixed, false trigger could happen to the conventional CL at a later juncture of the operational lifetime. On the other hand, for ZES LDAP, its first level of protection is innately insensitive to the gradual current increase, and its second level of protection cannot be falsely triggered as its threshold is set high.

In short, ZES LDAP's intelligent detection algorithm is able to unambiguously differentiate the SEL current from various behaviors of the operating current.

Third for **feature (d)**, ZES LDAP is radiation hardened by means of ZES' proprietary Radiation Hardening By Design (RHBD). ZES LDAP has been tested to be radiation hardened at least 300krad TID, and at least 110MeV-cm^2/mg for Single Event Effects, including SEL, SET, SEU etc.

ZES LDAP has been demonstrated to successfully protect various COTS ICs/SoCs both on ground and in outer space. These COTS include simple analog ICs like AD8629, mixed-signal ICs like AD7888, and complex digital SoCs like PIC16F688, ProASIC3, Kintex XC7K160T, SAMD21G18A, Zynq ZU3EG FPAGA-MPSoC etc. On grounds, it has been demonstrated that ZES LDAP is able to detect and subsequently protect every SEL event under heavy-ions and laser tests. In space, ZES LDAP has successfully achieved flight heritage in 4 satellites. In one of the missions, ZES LDAP

was directly benchmarked with the conventional CL, wherein one board embodied ZES LDAP protecting a COTS, and the other board, which is adjacently implemented, embodied the conventional CL protecting the COTS.
Over 12 months of mission time on a LEO CubeSat, the flight data showed that ZES LDAP successfully detected and protected the COTS from µSELs 41 times, and the conventional LCL didn't exhibit any protection at all – this observation was consistent with the ground testing data before the launch.

In summary, ZES LDAP offers unprecedented benefits of protecting advanced COTS ICs/SoCs from various current anomalies in space including µSEL, hence truly enable COTS into space missions.

3. Application of ZES100 LDAP (example: COTS FPGA)

ZES100 LDAP-IC is implemented on the power supply rail to monitor and protect the COTS devices (FPGA, MCU, GPU, Sensors, ADC, etc.,) from current anomalies in particular SEL.

Figure 5 depicts a general Power line connection to a COTS FPGA, however not every powerline is vulnerable to SEL. ZES' LDAP required only apply on the SEL-sensitive powerline(s).

The laser test is able to identify which powerline(s) is sensitive to SEL. In addition to SEL, data-flips/ soft-errors in memories caused by SET/SEU can also be evaluated and subsequently mitigated by **ZES' Voter-IC****.

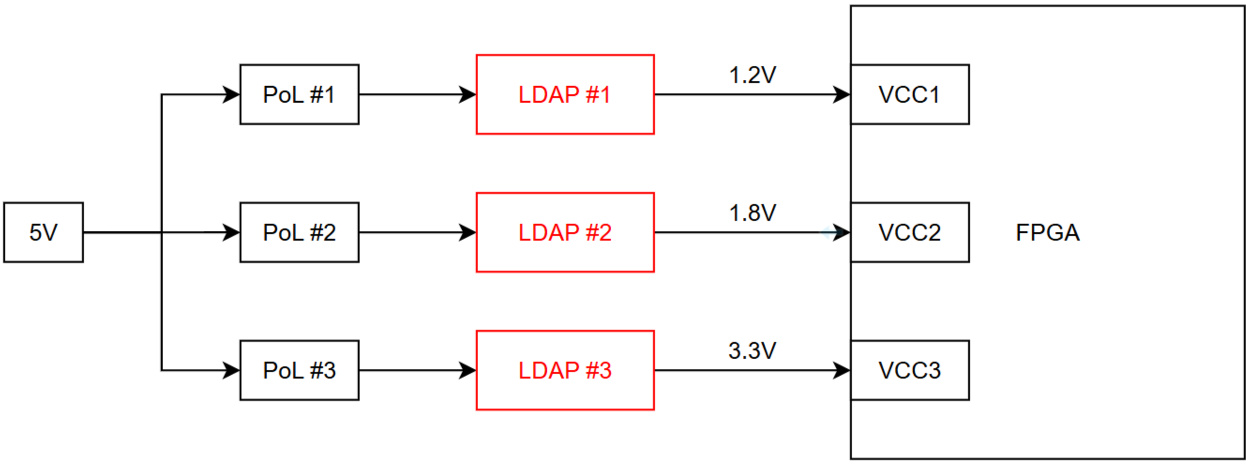


Figure 5 ZES' Recommended Solution of LDAP for COTS FPGA

** ZES' Voter-IC is ZES400 radiation hardened monolithic microchip with Triple-Modular-Redundancy (TMR) system.

Depending on various parameters that are embodied by radiation particles and COTS ICs, the SEL current profiles induced by each radiation hit can be different – this is confirmed by our observations of numerous radiation tests and laser tests of many different COTS ICs.

The conventional Current Limiter (CL), which offers SEL protection only when the SEL current exceeds a predetermined threshold (e.g. 3-4x of the nominal current), is grossly rudimentary and highly inadequate to handle the sophisticated and yet different SEL current profiles arising from advanced COTS ICs (e.g. FPGA) in modern satellites.

Conversely, ZES' solution, embodying Latchup Detection And Protection (LDAP), offers a very unique SEL detection and protection by means of intelligently monitoring the unique signature of the SEL current, and hence offering unprecedented advantages over the conventional Current Limiter solution. In the following, we will first explain why the employment of the conventional Current Limiter is flawed, followed by the benefits of ZES' LDAP solution. The description is based on a power reference design for an exemplary FPGA **Figure 5**, wherein the 5V bus is converted to 3 powerlines at different supply voltages (1.2V, 1.8V, 3.3V) and these powerlines are each protected by LDAP before connecting them to the FPGA.

4. Common issue with conventional Current Limiter Protection

During radiation and laser tests, it has been observed the power cycling by the conventional Current Limiter is inadequate for the removal of the SEL current in many advanced COTS ICs including FPGAs. Below **Figure 6(a)** depicts the SEL current when SEL occurs, wherein the SEL current flows from V_{DD} to Ground via the circuits latching up.
After the SEL current increases accumulatively until triggering the conventional Current Limiter. Subsequent to the triggering, V_{CC} is disconnected from the powerline and the SEL current stops to flow from the powerline to Ground. However, the SEL current is not removed.

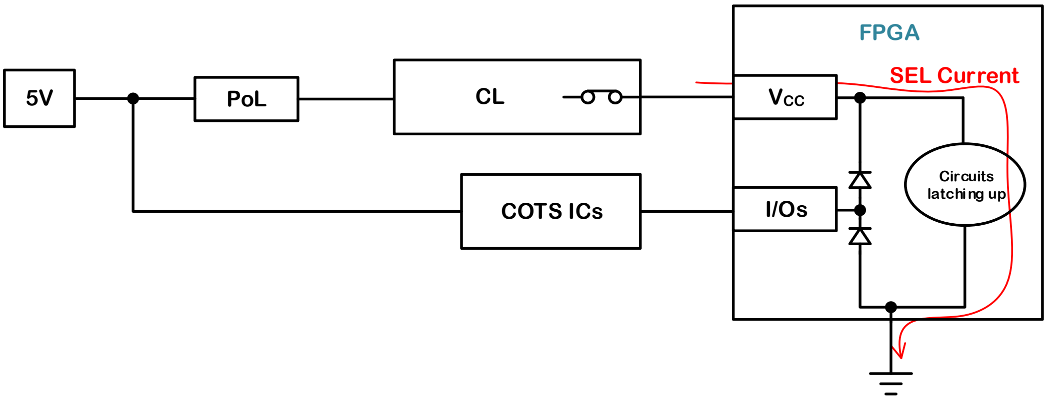


Figure 6(a)

Below **Figure 6(b)** depicts the SEL current after the conventional Current Limiter disconnects V_{CC} from the powerline, wherein the SEL current flows from I/Os sustained by preceding COTS ICs to Ground. In short, the conventional Current Limiter cannot protect the FPGA from SEL in this case.

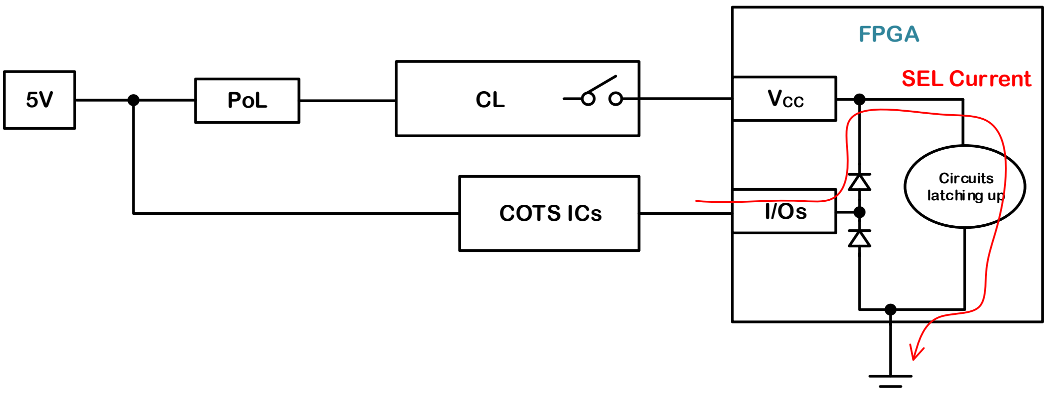


Figure 6(b)

Figure 6 SEL behavior via I/Os: (a) SEL occurs (b) SEL is not removed by Current Limiter

From the above case with the I/O issue, performing a laser test to evaluate ZES' solution integrated into conventional Current Limiter, as depicted in below **Figure 7**. When an SEL occurrence is detected by any LDAP, a flag signal is sent to OBC (On-Board-Computer) to demand the disconnection of 5V bus from other components. Note that ZES' solution may have several flag (Power Good, PG) signal variations depending on the complexity of FPGA.

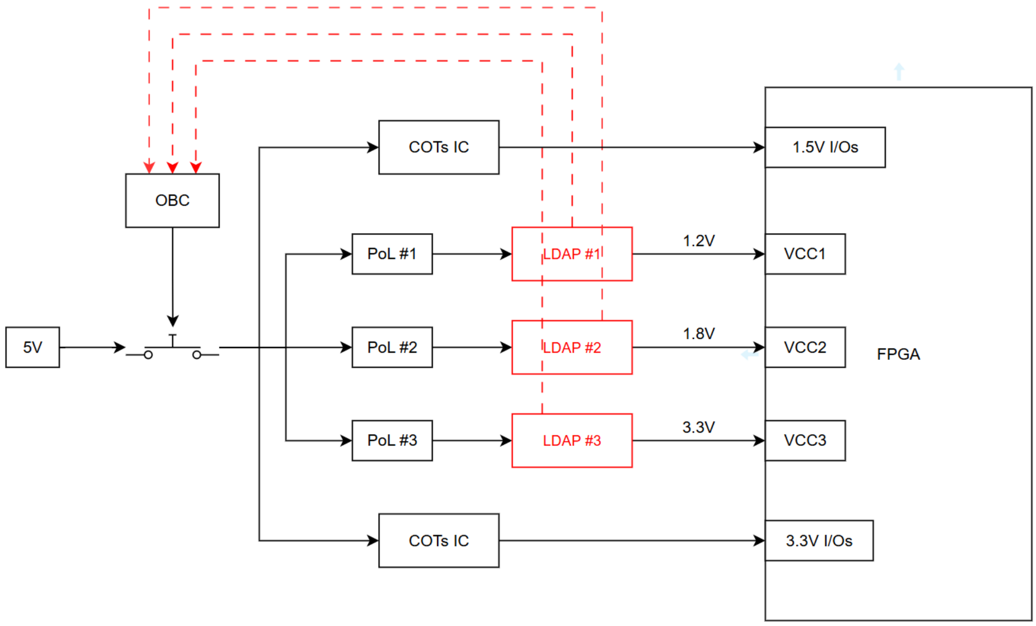


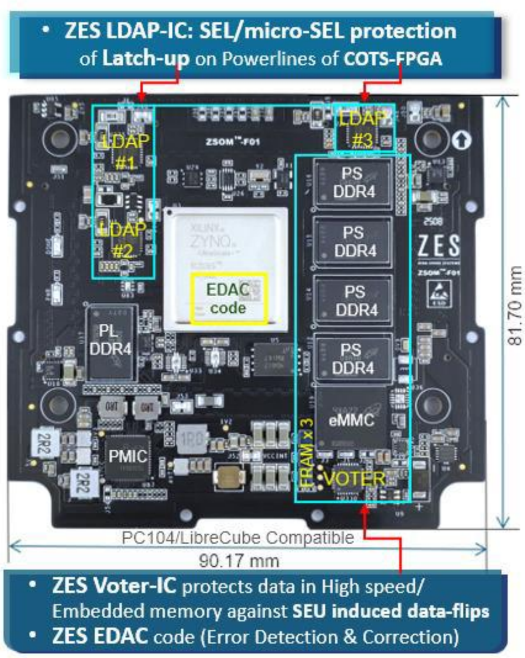
Figure 7 ZES' Recommended Solution of LDAP with OBC

Application Example: Protecting COTS-FPGA on SoM (ZSOM-F01)

ZES' Radiation Tolerant system-on-module **ZSOM-F01**, a high-performance FPGA system-on-module (SoM) based on AMD's Xilinx's Zynq UltraScale+ MPSoC (XCZU3EG- 1SFVC784I).

For the power reliability solution, three ZES100 Latchup-Detection-and-Protection (LDAP) Integrated Circuits (ICs) are applied to protect three power lines, i.e., 1.8V, 2.5V and 3.3V. The ZES100 LDAPs are used to detect Single-Event-Latchup (SEL), and if any SEL detected, to enable power-cycling to reset the entire ZSOM-F01, hence removing the SEL.

For the data integrity solution, a hardware-cum-software means is applied to protect the data associated with the eMMC NAND Flash, NOR flash memory, DDR4 memories, and the embedded block memory (BRAM) within the MPSoC FPGA. The hardware means is a Triple-Modular-Redundancy (TMR) memory consisting of a ZES400 Voter IC and 3pcs Ferro-electric Random Access Memories (FRAMs). The software means is a proprietary error detection and correction (EDAC) algorithm. The EDAC algorithm is configurable to protect data stored in various memories, and when necessary, to recover the corrupted data (if any) in those memories.



5. Implementation of ZES LDAP

The core of ZES LDAP consists of current sensing, an intelligent latch-up detector, recovery, and telemetry functions designed for high reliability system implementation.

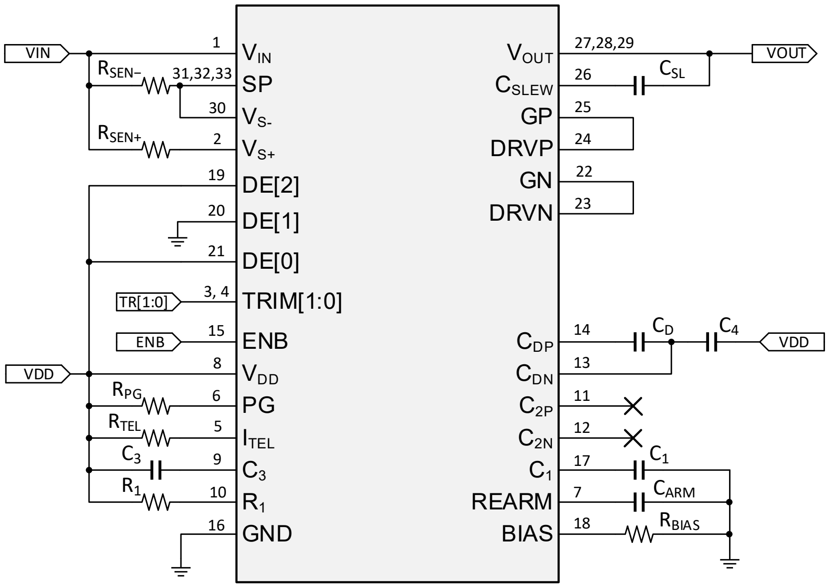


Figure 9 Typical application circuit implementation

Table 1 Typical values of implementation for ZES100 LDAP at the current limit of ~500mA, Current ratio of ~330

Symbol	Typical Value	Unit
R_{SEN-}	10 ±1%	mΩ
R_{SEN+}	3.3 ±1%	Ω
R_{PG}	100	kΩ
R_{TEL}	1 ±1%	kΩ
R_1	18 ±1%	kΩ
R_{BIAS}	470 ±1%	Ω
C_1	10 ±5%	nF
C_3	10 ±5%	nF
C_4	10 ±5%	nF
**C_D	10 ±5%	nF
C_{SL}	10 ±5%	nF
C_{ARM}	1 ±5%	nF

** For external P-channel MOFET application circuit, recommended capacitor C_D = 100 ±5% nF and verify the T_{OFF}.

5.1 Current Sensing

ZES LDAP has a built-in current sensor to read the current through V_{OUT}, i.e., the output/load current I_{OUT} as the sensed current I_{SEN} with a certain current sensing ratio. The current sensing ratio between I_{OUT} and I_{SEN} can be customized using R_{SEN-} and R_{SEN+} resistors by the following relationship.

$$r = \frac{I_{OUT}}{I_{SEN}} = \frac{I_{OUT,MAX}}{I_{SEN,MAX}} = \frac{R_{SEN+}}{R_{SEN-}}$$

The current sensing ratio depends on the load and the absolute maximum rating ZES LDAP internal sense current branch (~2mA). For example, for a Device Under Protection (DUP) with max. supply current, $I_{OUT,MAX}$ of 500mA, we can limit the maximum sensed current I_{SEN} to 1.52mA (additional derating) to obtain current sensing ratio of 330. If the R_{SEN-} resistance is set to be 10mΩ, then the R_{SEN+} resistance is 3.3Ω. It is recommended to design the minimum voltage drop across R_{SEN-} of 5mV.

The current sensing ratio accuracy may be affected by several factors such as parasitic resistance of PCB traces, resistors tolerance, internal offset, etc. To mitigate the impact of parasitic resistance of PCB traces, it is recommended that the PCB route from R_{SEN-} to V_{S-} (low current path for sensing) is isolated from the route from R_{SEN-} to SP (high current path).
Below
Figure 0 depicts a PCB layout example where the two paths are only connected together at one of the R_{SEN-} pads such that the voltage sensed by V_{S-} will be less affected by the voltage drop due to parasitic resistance of the PCB trace.

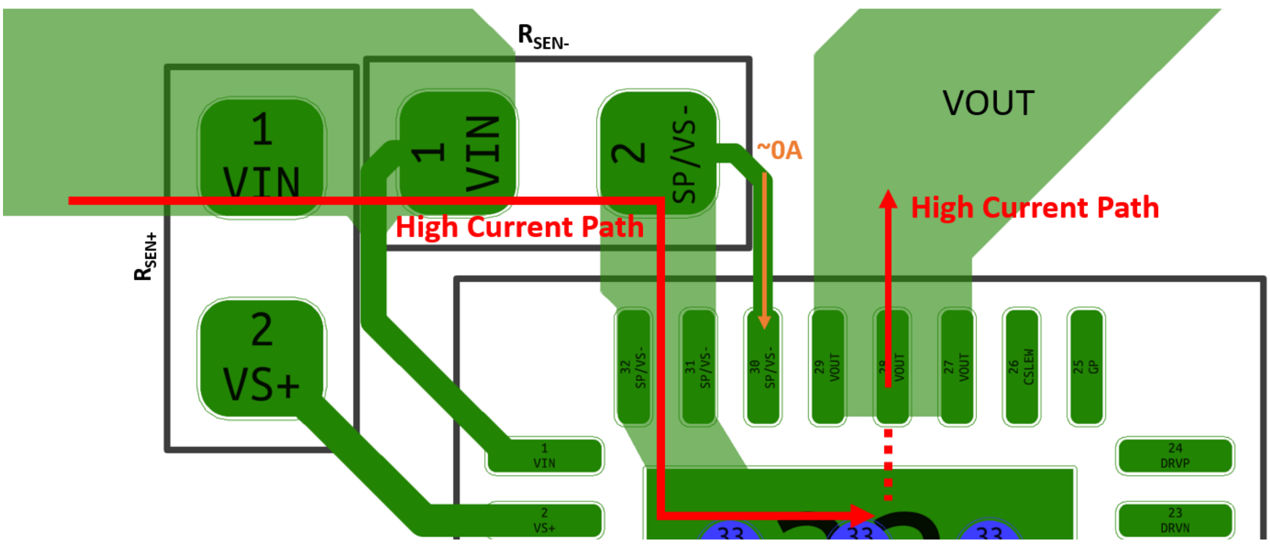


Figure 10 PCB layout recommendation for an optimized current sensing accuracy

5.2 Input and Output Capacitors

Integration of ZES LDAP into a system requires some consideration in the selection of both input capacitor C_{IN} and output capacitor C_{OUT} as these capacitors could induce sensitivity and reliability issues in detection of µSEL.

Figure 11 depicts the typical placement of C_{IN} and C_{OUT}. It is recommended to keep C_{OUT} to a low value (<<100nF) when possible. A high C_{OUT} may hinder the ZES LDAP's current sensing, as most of the DUP's dynamic supply current will be drawn from C_{OUT} instead of ZES LDAP. Furthermore, it is strongly recommended that C_{IN} >> C_{OUT} to prevent reverse bias current from V_{OUT} to V_{IN}.

For higher reliability, V_{OUT} should remain lower than V_{IN} such that there is not reversed bias internally.

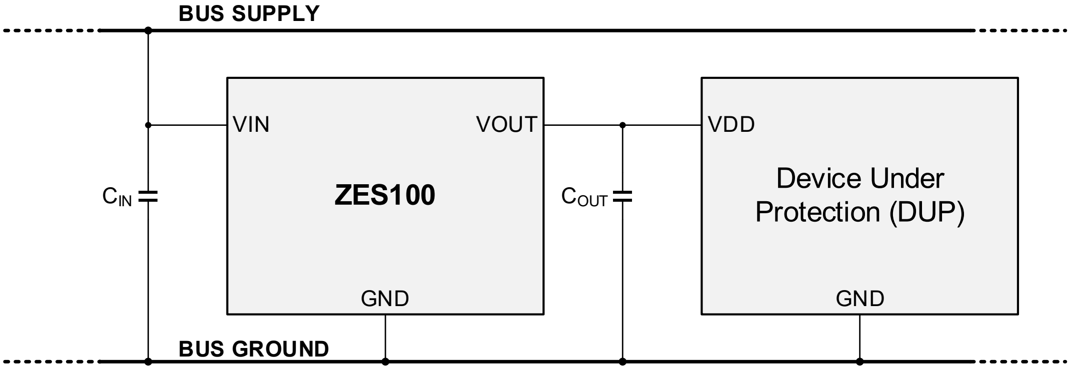


Figure 11 Input and output capacitors placement in a typical application circuit

5.3 External Control (MCU/FPGA) of Power Cycling (counting SEL occurrence)

In some applications, there is a need for extra flexibility in controlling the power cycling sequence as it could be disruptive to other parts in a system. There are several ways to configure ZES100 for such applications.

Figure 12 depicts an example of ZES100 configuration where the recovery sequence (power cycling) is externally controlled by a microcontroller (MCU) unit. The DRVN pin serves to provide a flag signal to the MCU. DRVN = "1" means an SEL/overcurrent is detected, while DRVN = "0" means no overcurrent/SEL is detected.

When there is SEL/overcurrent flag signal detected by MCU, the MCU can count the number of SELs and delay the power cycling until the suitable time to activate the power cycle.

The MCU can activate the power cycling through both O1 and O2 (Output1 and Output2) pins connected to ZES100 GP and GN pin. GP and GN pins are the gate pin of the internal power PFET and NFET switches, respectively.

O1 = “0” means turn on internal PFET and O2 = “0” means turn off internal NFET switches, to turn ON V_{OUT}.

O1 = “1” means turn off internal PFET and O2 = “1” means turn on internal NFET switches, to turn OFF V_{OUT}.

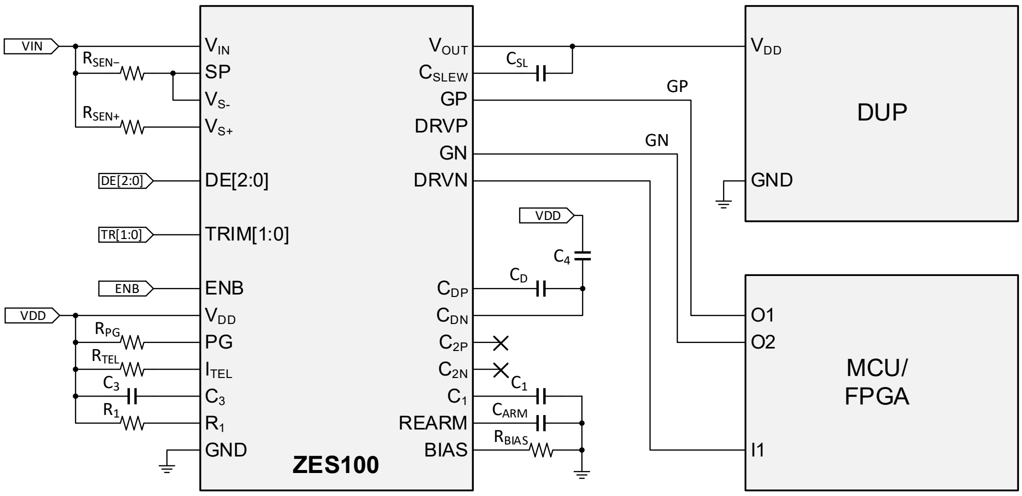
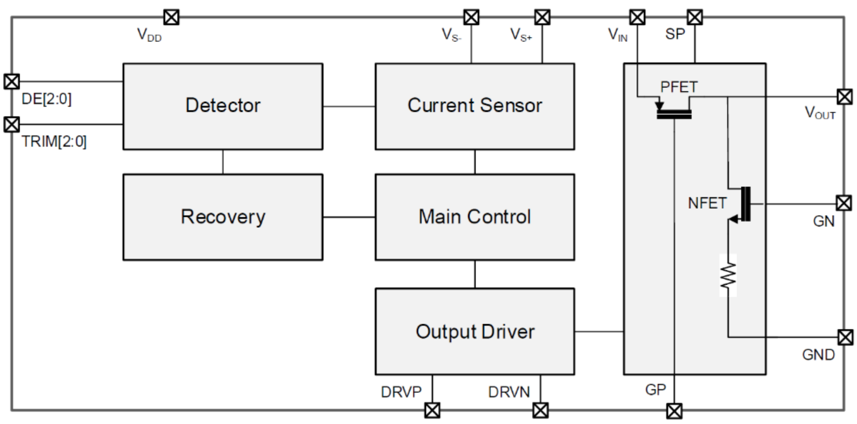


Figure 12 An example of ZES100 configuration with external control of power cycling

In the event, when the LDAP pull-down switch (internal NFET) is not required/necessary, the NFET switch can be disabled by connecting GN pin to GND.



ZES100 LDAP-IC Simplified Block Diagram

5.4 Limit to Single Power Cycle

In some applications, during the over-current state there is a need to just have a single power cycle instead of having power cycling sequence repeated until the overcurrent state is removed.

Figure 13 depicts an example of ZES100 configuration where the recovery sequence (power cycling) is limited to just one single cycle. The PG pin serves to provide a flag signal to the On-board-computer (OBC). The OBC will disable the ENB pin when there is PG negative pulse detected. This will limit the power cycling sequence from repeated until the overcurrent state is removed.

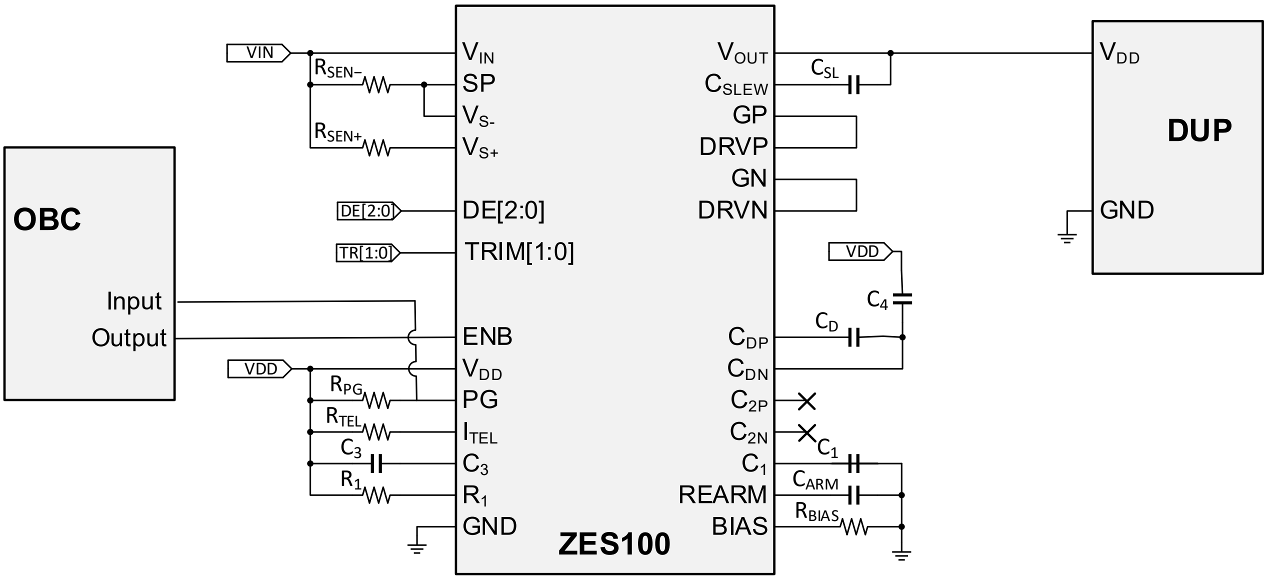


Figure 13 An example of ZES100 configuration with Single power cycle

5.5 External Power Switches (for higher I_{OUT} >500mA)

The ZES100 LDAP has a built-in power PFET switch, and a pull-down NFET switch (in series with a 50 Ω resistor). Both the built-in power switches are de-rated and their gates are accessible through GP and GN, respectively. The max drain-source current of the power PFET is 500mA at 125°C. These power switches can be driven by ZES100's drivers DRVP and DRVN pins. To use the built-in power switches, simply connect DRVP to GP, and DRVN to GN as depicted in above **Figure 9**.

The ZES100 also supports the use of an external power switch (P-Channel MOSFET) to deliver higher I_{OUT} (>500mA) to load. **Figure 14** depicts an example circuit configuration to implement ZES100 with an external power P-Channel MOSFET*.

** Infineon IRHLNA797064, IRHLNA793064 Radiation-Hardened 60V, 56A P-channel Power MOSFET.*

Recommendation for the selection of external switch, the Gate-Source Threshold Voltage $V_{gs(th)} > V_{IN} – 0.2V$.

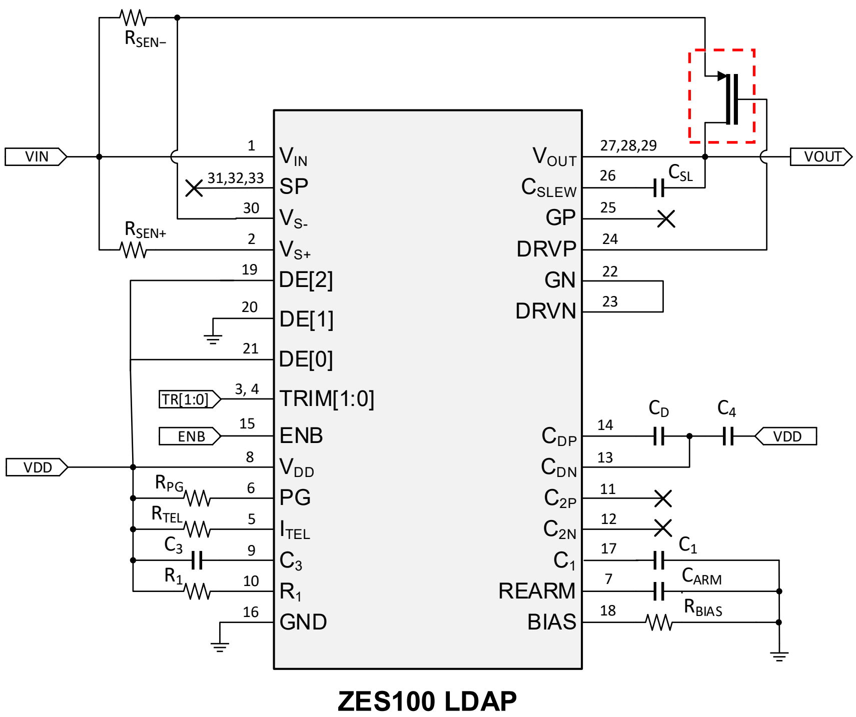


Figure 14 Circuit configuration to implement ZES100 with an external power switch (PFET)

Appendix

Revision History

Revision No.	Notes	Date
Rev 1.0	Preliminary version	Sept, 2022
Rev 3.1	Preliminary version	Sept, 2023
Rev 3.2	Preliminary version	Nov, 2023
Rev 3.3	Initial Release	Oct, 2024
Rev 3.4	Replace 0.9V with 1.2V (Figure 7)	Jul, 2025
Rev 3.5	For pin-description PG/Sync; Changed to PG pin	Nov, 2025

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