Voter Module ZM-VF01A

Datasheet
Preliminary V1.0 Mar .'25

Radiation-Hardened Voter Module
Triple-Modular-Redundancy Voter-IC + FRAM

Enabling Advanced Commercial-Off-The-Shelf (COTS) to 'Space-Grade'

Detection & Correction of SEU induced Soft-errors in GPU/FPGA/MCU Memories

Overview

ZM-VF01A is a Voter-module with **radiation-hardened Voter-IC (ZES400)** integrated with Triple-Modular-Redundancy (TMR) Ferroelectric Random Access Memory (FRAM) 1M-bit (3pcs) together with ZES Error-Detection-and-Correction (ZEDAC) C-code (software) for **Single-Event-Upset (SEU) protection of data stored in the embedded memory** (e.g., initialization data, config data, user data, etc.) & External high-speed memories (DDR).

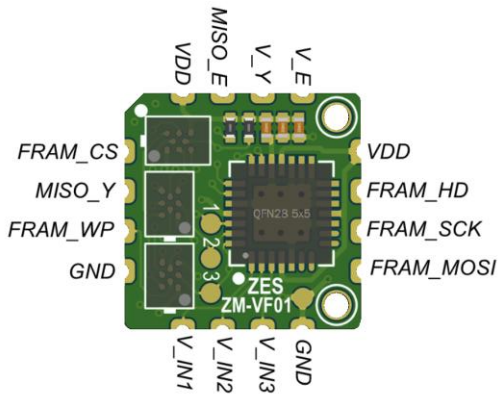
The ZES400 Voter embodies 4-channel voting circuits where one of the channels is used to vote the outputs of the FRAMs. An additional voter channel is available for supporting TMR for another signal where necessary. The ZM-VF01A features ultra-low error, suitable for storing critical data storage and/or supporting ZEDAC algorithms.

Compact form factor Module (11.8mmx 11.8mm) can easily be plug-in to the existing COTS sub-system (MCU/FPGA/GPU) with minimal design changes to payloads.

Applications

- Low power embedded applications for CubeSat payloads for Low-Earth-Orbit (LEO)
- Scientific data processing payloads (Image-sensing, including AI and/or edge-computing)
- Earth Observation payloads (e.g., Camera/ SAR/ sensor applications)
- Telemetry/data communication applications
- Low error-rate data protection applications
- Instrumentation and control for high reliability applications
- SEU protection of existing MCU/FPGA/GPU subsystems with Plug-in module design

ZM-VF01A Voter Module (11.8 x 11.8mm)



Key Features

- High Radiation Performance ZES400 Voter:
  Total Ionizing Dose (TID): 300krad (Si)
  Single-Event-Latchup (SEL): 110MeV-cm^2/mg
  Single-Event-Upset (SEU): 83MeV-cm^2/mg
- FRAM with inherent SEU radiation hardness
- Operating voltage: 1.8V ~ 3.6V
- Operating Temperature: -40^{o}C to 85^{o}C
- SPI interface with the FRAMs
- Additional voter channel available for enabling TMR for another customized signal
- TID (Module): TBD
- Proton test (Module): TBD
- Laser tested FRAMs: no SEL up to 5,500pJ Laser energy
- Proprietary error-detection-and-correction (ZEDAC) C-code for detecting/correcting multiple errors in embedded/Hi-speed memories in MCU/FPGA/GPU
  - 2,000x less soft error than Single-Error-Correction-Double-Error-Detection (SECDED)
- Compact form factor, Plug-in module type (Size: 11.8mm x 11.8mm)

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1 Overview

ZM-VF01A is a Voter-module with radiation-hardened Voter-IC (ZES400) integrated with Triple-Modular-Redundancy (TMR) Ferroelectric Random Access Memory (FRAM) three pieces 1M-bit FRAMs implemented in TMR. The ZES400 voter embodies 4-channel voting circuits where one of the channels is used to vote the outputs of the FRAMs. An additional voter channel is available for supporting TMR for another signal where necessary. The ZM-VF01A features ultra-low error, suitable for storing critical data storage and/or supporting ZES error-detection-and-correction (ZEDAC) algorithms.

1.1 Features

- Radiation-hardened ZES400 Voter adopted (Total Ionizing Dose (TID) @ 300krad (Si), Single-Event-Latchup (SEL) @ 110MeV-cm^2/mg and Single-Event-Upset (SEU) @ 83MeV-cm^2/mg)
- FRAM (part number: MB85RS1MT x 3pcs) with inherent SEU radiation hardness
- Operating voltage: 1.8V ~ 3.6V
- Temperature: -40^{o}C to 85^{o}C
- SPI interface with the FRAMs
- Additional voter channel available for enabling TMR for another customized signal
- Overall Total Ionizing Dose (TID): TBD
- Overall proton test: TBD
- Laser test on FRAMs – no Single-Event-Latchup (SEL) @ up to 5.5nJ laser energy

1.2 Block Diagram

Fig. 1 depicts the simplified diagram of ZM-VF01A, showing ZES400 and FRAM components and their interface signals/connections. The primary inputs/outputs are shown; their pin definitions are delineated in Table 1 of Section 2.1.

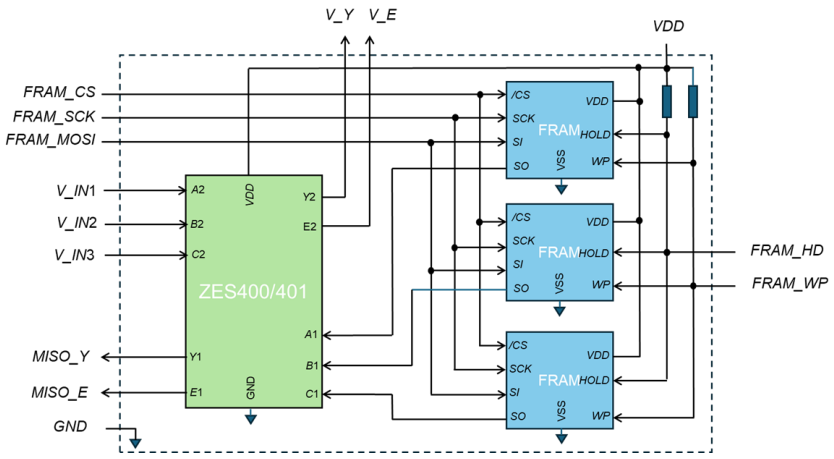

Fig. 1: The simplified block diagram of ZM-VF01A

1.3 Ordering Information

Ordering Information

PART No.	Size
ZM-VF01A	11.8 mm x 11.8 mm
ZEDAC Algorithm	Software

For further details, price, delivery, and ordering information please contact info@zero-errorsystems.com

2 Signal/Pins and Operation Control

Fig. 2 depicts the pin assignment of ZM-VF01A.

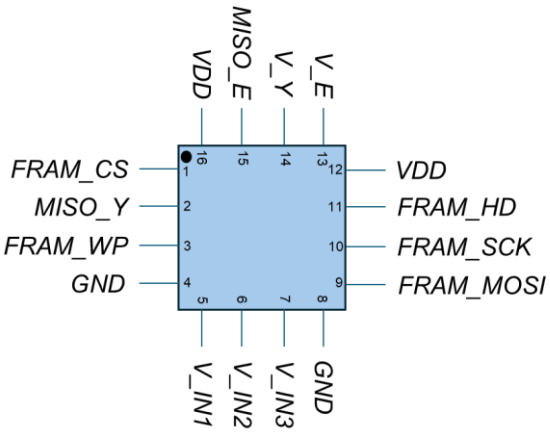

Fig. 2: Pin assignment of ZM-VF01A

2.1 Module Input/Output (I/O)

Table 1: **I/O Signals**

S/N	Pin Name	I/O Type	Pin Description	Remark
1	*FRAM_CS*	Input	FRAM Chip Select pin	See Figs. 1 and 2 for the pin locations
2	*MISO_Y*	Output	FRAM Serial Data Output pin (through ZES400)	
3	*FRAM_WP*	Input	FRAM Write Protect pin (with a pull-up resistor onboard)	
4	*GND*	Ground	Ground pin	
5	*V_IN1*	Input	ZES400 Voter Channel Input 1 pin	
6	*V_IN2*	Input	ZES400 Voter Channel Input 2 pin	
7	*V_IN3*	Input	ZES400 Voter Channel Input 3 pin	
8	*GND*	Ground	Ground pin	
9	*FRAM_MOSI*	Input	FRAM Serial Data Input pin	
10	*FRAM_SCK*	Input	FRAM Serial Clock pin	
11	*FRAM_HD*	Input	FRAM Hold pin (with a pull-up resistor onboard)	
12	*VDD*	Power	Supply Voltage pin	
13	*V_E*	Output	ZES400 Voter Channel Output for Error pin	
14	*V_Y*	Output	ZES400 Voter Channel Voted Data Output pin	
15	*MISO_E*	Output	FRAM Serial Data Output Error pin (through ZES400)	
16	*VDD*	Power	Supply Voltage pin	

2.2 FRAM SPI Operation Control

Fig. 3 depicts the SPI control modes for accessing the FRAMs. Please note that for each operation (e.g., write or read), the three FRAMs are written/read simultaneously.

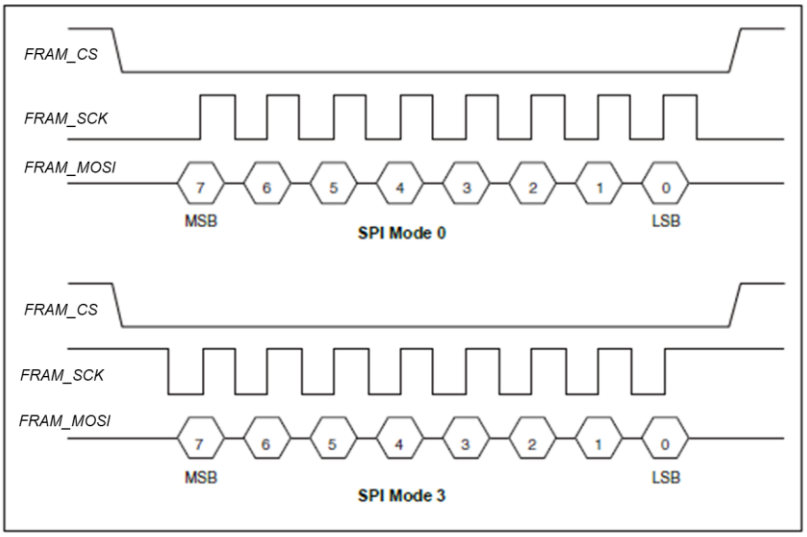

Fig. 3: The SPI modes for accessing FRAMs

2.3 FRAM Access Timing Diagram

Figs. 4 (a) and (b) depict the access timing diagrams for the read operation and write operation, respectively.

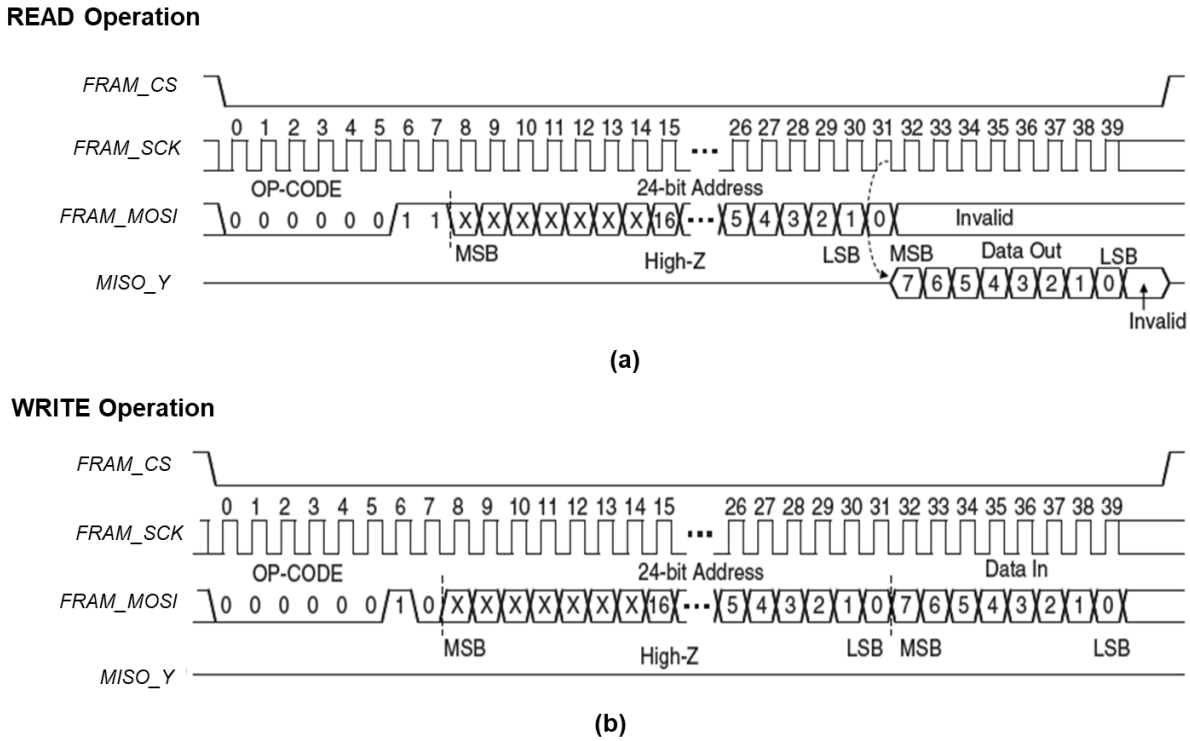

Fig. 4: The access timing diagram: (a) read operation, and (b) write operation

2.4 Voter Channel Control

Table 2 tabulates the truth table of the voter channel.

Table 2: Voter Channel Truth Table

V_IN1	*V_IN2*	*V_IN3*	*V_Y*	*V_E*
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	1
1	0	0	0	1
1	0	1	1	1
1	1	0	1	1
1	1	1	1	0

3 Technical Specifications

3.1 Recommending Operating Conditions

Table 3 tabulates the recommended operating conditions for operating ZM-VF01A.

Table 3: Recommended Operating Conditions

Symbol	Parameter		Min	Typ	Max	Unit
T	Temperature range		-40	-	+85	℃
V_{DD}	Voltage supply of the module		1.8	3.3	3.6	V
V_I	Input voltage		0	-	V_{DD}	V
V_O	Output voltage		0	-	V_{DD}	V
f	Maximum frequency (RT*, 3.3V, 4.75pF*)		-	-	20	MHz
I_{CC}	Max. Power Typ. @ RT*, 3.3V, 20MHz FRAM Read/Write, 4.75pF* Max. @ 85℃, 3.6V, 20MHz FRAM Read/Write, 4.75pF*		-	TBD	TBD	mA
V_{IH}	High-level input voltage	V_{DD}=1.8±10% V	1.26	-	-	V
		V_{DD}=3.3±10% V	2.32	-	-	V
V_{IL}	Low-level input voltage	V_{DD}=1.8±10% V	-	-	0.54	V
		V_{DD}=3.3±10% V	-	-	0.99	V
I_{OH}	High-level output current	V_{DD}=1.8±10% V	-	-	-2	mA
		V_{DD}=3.3±10% V	-	-	-4	mA
I_{OL}	Low-level output current	V_{DD}=1.8±10% V	-	-	2	mA
		V_{DD}=3.3±10% V	-	-	4	mA
t_r, t_f	Input rise or fall time (10% to 90%)	V_{DD}=1.8±10% V	-	-	1000	ns
		V_{DD}=3.3±10% V	-	-	400	ns

*Assuming capacitance due to PCB traces is negligible *RT: Room Temperature

3.2 Reliability Tests

The module reliability test results are summarized below in Table 4.

Table 4: Reliability Tests

Parameter	Condition	Value*	Units
Proton Testing	Proton fluence = TBD	TBD	MeV
SEU	Cross-Section @ Proton - TBD	TBD	cm^2
Total Ionizing Dose (TID)	Cobalt-60 @ TBD	TBD	Krad
SEL @ Laser	Laser Testing on FRAMs	5,500	pJ

* The results are the characterized values during the test.

3.3 Physical Dimensions

Fig. 5 depicts the physical outline dimension for ZM-VF01A.

Fig. 6 depicts the recommended footprint while integrating ZM-VF01A into another module.

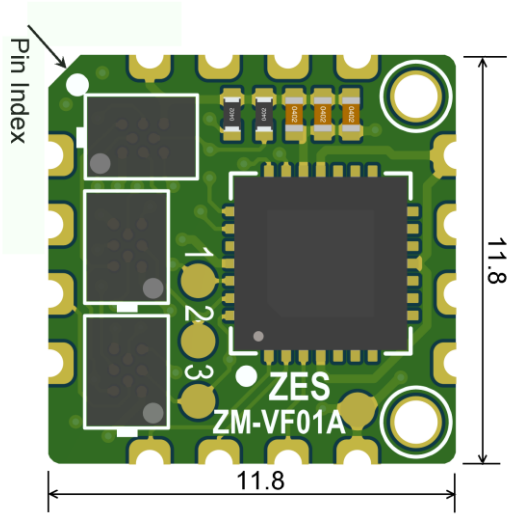

Fig. 5: Physical outline dimension

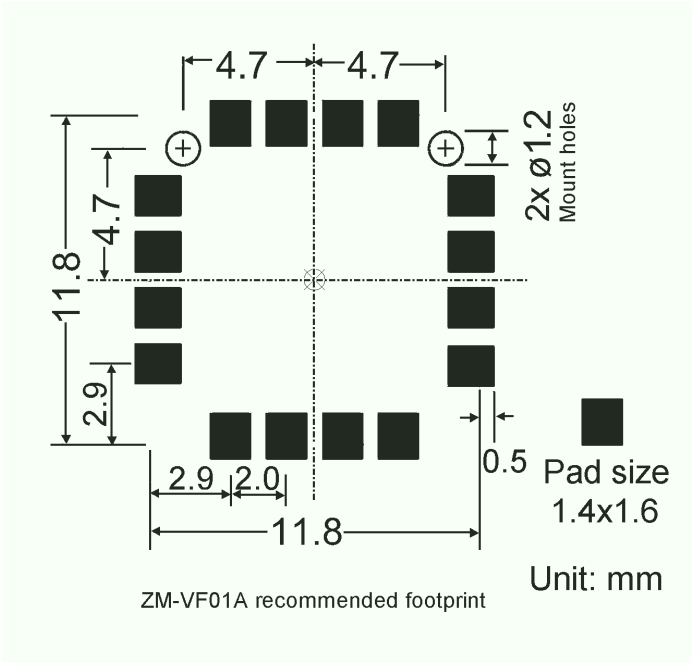

Fig. 6: Recommended footprint

4 Recommended Interface

Fig. 7 depicts the recommended interface connection when a microcontroller (MCU) or a Field-Programmable-Gate-Array (FPGA) is connected to ZM-VF01A via an SPI interface. Please note that the pull-up resistor R1 and the pull-down resistor R2 could be optional if the MCU or FPGA can provide sufficient current drive to drive ZM-VF01A. If not, please refer to the datasheet of the MCU/FPGA/GPU to provide appropriate R1 and/or R2 values to drive ZM-VF01A.

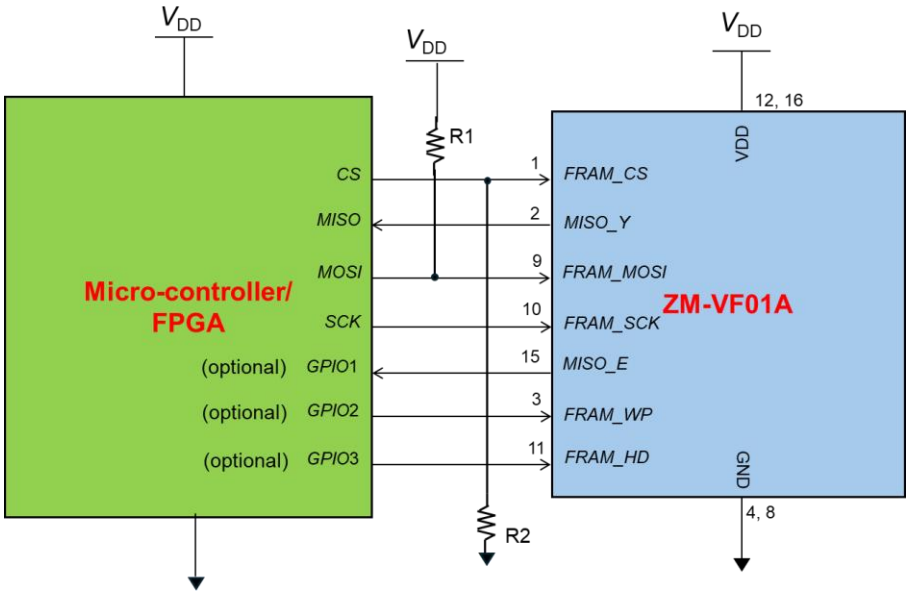

Fig. 7: Recommended interface connection between MCU/FPGA and ZM-VF01A. The pull-up resistor R1 and pull-down resistor R2 could be optional.

5 Application Examples

5.1 Hardware/software co-solution for enabling ZES Error Detection-and-Correction (ZEDAC) algorithm

ZM-VF01A is integrated with the ZES error-detection-and-correction (ZEDAC) algorithms to enable data protection virtually for any memories (e.g., eMMC or DRR4). Fig. 8 briefly depicts the interface setup where a processing unit embodying either the MCU or FPGA. The processing unit is interfaced with an external memory and ZM-VF01A. The external memory could be a Commercial-Off-the-Shelf (COTS) memory (e.g.., eMMC or DDR4) whose data need to be protected. The ZEDAC algorithm is executed within the MCU/FPGA, providing the encoding/decoding process. The ZM-VF01A and the ZEDAC algorithm collectively serve as hardware/software co-solution to reduce the soft-error (e.g., bit flips) in the external memory. The hardware/software co-solution provides 50x better error-rate than the hardware-only solution, and 2,000x less soft errors than Single-Error-Correction-Double-Error-Detection (SECDED)

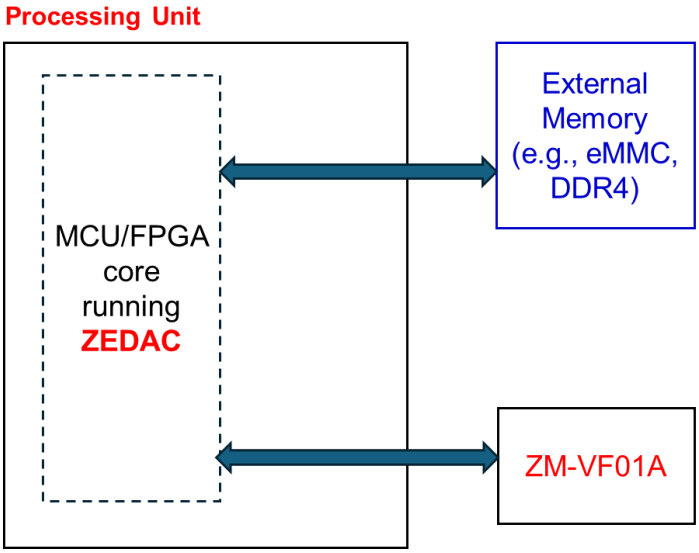

Fig. 8: Setup for enabling hardware/software co-solution to feature ultra-low soft-error rate (in part using ZM-VF01A and ZEDAC algorithm)

5.2 Add-on Connector for Interfacing a System with SPI Ports

ZM-VF01A can be mounted to a customized add-on connector board which can be interfaced with a system/subsystem via the GPIO pins. Fig. 9 depicts an example where the add-on connector is designed to embody the ZM-VF01 module, and to have a 40-pin interface compatible with a Nvidia Nano Orin GPU sub-system. With the add-on connector, the ZM-VF01 is inherently connected (via the SPI ports) to the MCU of the Nvidia Nano Orin system. If necessary, the ZEDAC algorithm can be easily executed in the MCU, checking/recovering the data using the MCU and the ZM-VF01. The data could be embedded SRAMs within the MCU, or the dedicated eMMC/DDR memories within the Nvidia Nano Orin sub-system.

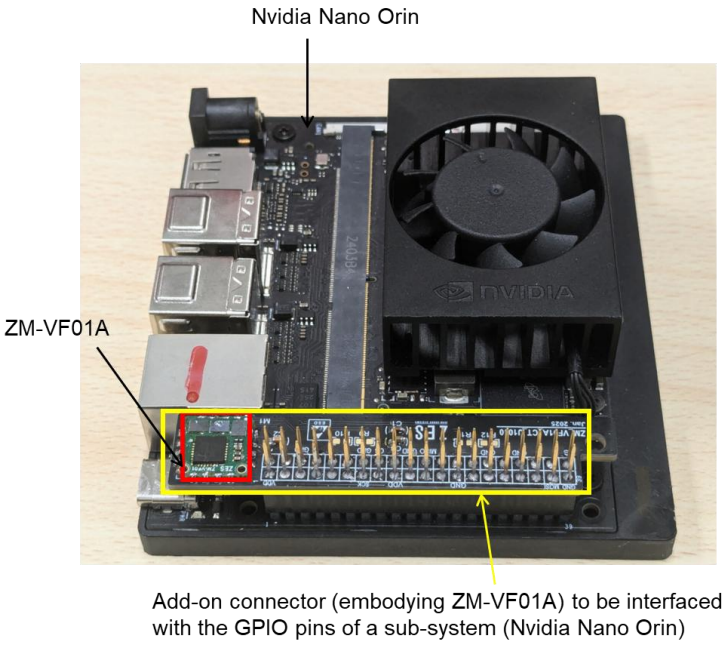

Fig. 9: An example: ZM-VF10A mounted on a connector board which is interfaced with a Nvidia Nano Orin sub-system (via 40-pin GPIOs)

Similarly, the add-on connector board can be customized for other systems/sub-systems such as Raspberry Pie systems/sub-systems.
For more information about the add-on connector, please contact info@zero-errorsystems.com

5.3 Critical data storage

ZM-VF01A can be used to store critical data such as the boot programs, critical configuration data, AI-model data, critical output data, and critical operational status information for satellite applications or high reliability applications. Please note the memory capacity limit is 1M-bit.

5.4 Voter Channel Application

ZM-VF01A has an additional voting channel which can enable TMR for two sub-systems. Fig. 10 depicts an example how the data can be transferred, via ZM-VF01A, between the two sub-systems A and B. In the sub-system A, three sub-circuits T1, T2 and T3 generate three same signals T_a, T_b, and T_c which are voted by ZM-VF01A to generate a voted ouput T_y. The three sub-circuits T1, T2 and T3 are usually the same. The voted output T_y is virtually SET-hardened. The voter output T_y is virtually error-free provided that the error possibility to have two errornos signals (out of the three signals T_a, T_b, and T_c) is assumed to be very low. The error indication signal T_e can be used to allert the sub-system B, indicating that at least one of the three signals T_a, T_b, and T_c is different.

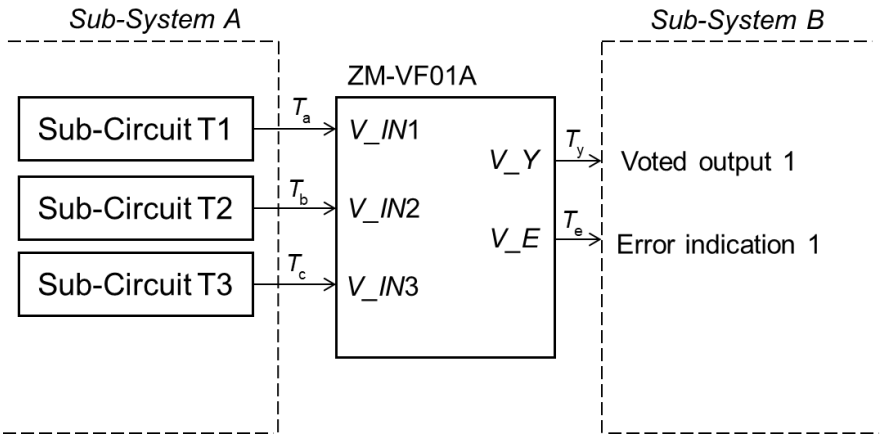

Fig. 10: TMR application example using the voter channel

6 Revision History

Version	Description	Date
V1.0	Preliminary datasheet	Mar-2025

7 Legal

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