ZES
ZERO-ERROR SYSTEMS

Introduction to ZES Solutions & Applications

Zero-Error Systems Pte. Ltd.

Enabling Commercial-Off-The-Shelf Integrated Circuits into Space

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Table of Contents

Introduction to ZES Solutions

This document presents ZES' enabling solution to protect COTS ICs from Single Event Effects (SEE) – enabling COTS ICs into space. Figure 1 below depicts a simplified block diagram of ZES' enabling solution, that provides unprecedented both **Power Reliability** and **Data Integrity**.

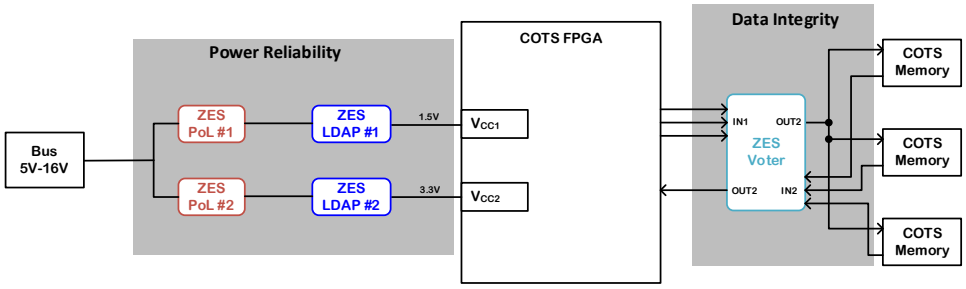


Figure 1 Exemplar diagram of ZES' enabling solution for a COTS FPGA and COTS memories in space

The primary constituents of ZES' enabling solution are: (1) the radiation-hardened Latchup-Detection-And-Protection (LDAP), (2) the radiation-hardened Point-of-Load (PoL), and (3) the radiation-hardened Voter. Collectively, they significantly enhance **Power Reliability** and **Data Integrity** of the COTS FPGA and COTS memories. Specifically, the LDAP mitigates Single-Event-Latchup (SEL), which could otherwise damage (i.e. burning by generating heat) COTS permanently, hence significantly enhancing **Power Reliability**. The PoL provides stable and uninterrupted voltage supplies to the COTS FPGA; innate redundancy is possible depending on the configurations. In view of these, both **Power Reliability** and **Data Integrity** of the COTS FPGA are enhanced. The Voter serves to substantially mitigate Single-Event-Upsets (SEU) in both the COTS FPGA and the COTS memories, hence significantly enhancing **Data Integrity** of the entire computation system. The LDAP, PoL and Voter will now be delineated in turn.

Radiation-Hardened Latchup Detection and Protection (LDAP)

The effects of radiation can be severe in space arising from occasional heavy-ion and/or proton strikes in Low Earth Orbit (LEO) to frequent strikes in deep space. Consequently, the reliability of new- and next-generation satellites that are largely implemented with COTS ICs would certainly be compromised. Although some of COTS ICs have been successfully applied in Low Earth Orbit (LEO), the choice of these COTS ICs is very limited, and their lifetime in space is largely unknown. Further, a careful risk assessment is necessary, including identification of vulnerabilities COTS IC (particularly to SEL), and thereafter appropriate realizations to mitigate the said radiation effects. Note that SEL is well-recognized as one of the most critical mechanisms of mission failure.

ZES' solution enables **Power Reliability** when applying COTS ICs in new- and next-generation satellites – by adopting and implementing ZES' LDAP to protect COTS ICs from the destructive SEL. ZES's LDAP embodies proprietary technology (***2 granted patents***) that enables intelligent detection of and protection against SEL for virtually all COTS ICs. Specifically, ZES's LDAP has been demonstrated its efficacy to be able to detect every SEL occurrence and protect the COTS ICs (analog, micro-controller, FPGA and mixed-signal microchips) and without false triggering under irradiation tests, including laser and heavy-ions in a cyclotron. The degree of protection ZES's LDAP provide is unprecedented – >**100× better than** the general current limiter. Depending on the actual implementations, this superiority leads to at least 7

years lifetime enhancement (depending on the orbits). In short, for the first-time, virtually **all COTS ICs** can be safely applied into new and next-generation satellites. The details of why and how to use ZES' LDAP is provided in Appendix A.

Radiation-Hardened Point-of-Load (PoL)

Power management/distribution subsystem (including PoLs) is one of the most critical subsystems in satellites, because it must be highly power-efficient, yet highly **reliable** including radiation-hardened, and where possible, offer redundancy without excessive hardware or form-factor overheads. Unfortunately, COTS PoLs are not only non-radiation-hardened, rendering them largely inapplicable, but also inflexible and suffer from other shortcomings – see later. Conventional Radiation-hardened PoLs, on the other hand, are inflexible, not power-efficient and do not offer redundancy.

ZES provides a unique PoL solution for new- and next-generation satellites – by adopting and implementing ZES' PoL which is not only radiation-hardened, but also flexible, and features higher power-efficiency, collectively achieving **Power Reliability** and **Data Integrity**. These features are particularly pertinent as power management is the primary mechanism of mission failure.

ZES PoL embodies a proprietary architecture (***4 pending patents***), offering several unique attractive advantages over COTS PoLs. First, ZES' PoL always operates at its maximum power efficiency over a wide loading range vis-à-vis COTS PoL high power-efficiency only in a small operating range (e.g. at high loads). This feature is highly advantageous to new- and next-generation satellites in view of their form-factor, limited energy resource and diverse operating range. Second, ZES' PoL is radiation-hardened and is inherently insensitive to Single-Event-Latchup and Single-Event-Transients, thereby offering **enhanced Power Radiality** and **Data Integrity**. Third, depending on the implementations, ZES' PoL allows innate **redundancy** by paralleling multiple PoLs within the same microchip package or on the same board. Fourth, ZES' PoL can be realized with very small output inductance – an unprecedented **10× lesse**r – hence a significantly smaller Printed-Circuit-Board footprint, i.e., much smaller form-factor. Fifth, ZES' PoL allows an unprecedented high step-down ratio, e.g., 20V-to-1V without compromising any other parameter. Sixth, ZES PoL offers rapid transient response, allowing fast transition between light load and heavy load. When compared to present-day radiation-hardened PoLs, ZES PoLs offer the aforesaid first, third to sixth advantages. ZES PoL has demonstrated its efficacy and advantages under irradiation tests, including laser and heavy-ions in a cyclotron.

Radiation-Hardened Voter

As commercial-off-the-shelf (COTS) devices are not space-grade or radiation-hardened, they suffer from severe data soft-errors under radiation environments, including Single-Event-Transients and Single-Event-Upsets. The common practice to enable COTS devices to be more resilient is to include redundancy, typically by physical redundancy at the cost of hardware overheads. To enable an effective hardware redundancy, the critical assumption is that the voter circuit (serving as a judge to check the outputs of redundancy) must feature an ultra-low error-rate.

ZES' voter is designed to support a triple-modular-redundancy architecture to accept multiple outputs from COTS devices, and is capable of filtering erroneous outputs and/or possibly correcting erroneous outputs of the COTS devices. ZES' voter is best applied to the circuit modules for communication protocols, including UART, SPI and I^2C. ZES' voter is realized based on ZES's digital Radiation-Hardened-By-Design (RHBD) technologies (patents pending).

ZES' RHBD technologies are advantages for realizing digital circuits for high radiation hardness and yet low power-delay-area overheads. Of particular interest, the sequential circuits (e.g., registers)

embodying ZES' RHBD technologies have an unprecedented 3.5× lower power-delay-area overheads than state-of-the-art radiation-hardened approaches – an imperative consideration for System-on-Design (SoC) designs in view of the severe resource constraints of new- and next-generation satellites. Circuits embodying ZES' RHBD technologies have been verified under irradiation tests, including laser and heavy-ions in a cyclotron.

Summary

In summary, the abovementioned design and realization of protecting COTS ICs provides a unique enabling solution for an **unresolved REAL need** in the space industry. It provides **unprecedented degree-of-freedom** for the selection of advanced COTS ICs for space applications – enabling cheaper, yet more intelligent and sophisticated new- and next-generation satellites with desirable **Power Reliability** and **Data Integrity**. Specifically, **many state-of-the-art ICs that cannot be applied in space can now be applied**. We believe that this solution, embodying LDAP, PoL and Voter will be a **technological enabler** for the space industry and the **de-facto industry-standard** protection interface module for COTS in new- and next-generation satellites.

Latch-Up Protection & Detection (LDAP) in details

Radiation Hardened LDAP: ZES's Latchup Detection and Protection Solution – Enabling Advanced Commercial-Off-The-Shelf (COTS) ICs into Space

Overview

It is well known that COTS ICs are sensitive to various radiations effects in space. Amongst the various radiation effects, Single Event Latchup (SEL) has the most detrimental effect, because it can substantially reduce the lifetime of COTS ICs for the best or permanently destroy COTS ICs for the worst. Although the mechanism of SEL is well understood, the SEL behaviour of modern COTS ICs (e.g. FPGA) can be very sophisticated. Depending on various parameters that are embodied by radiation particles and COTS ICs, the SEL current profiles induced by each radiation hit can be very different – this is confirmed by our observations of numerous radiation tests and laser tests of many different COTS ICs.

The current limiter, which offers SEL protection only when the SEL current exceeds threshold (i.e. 3-4× of the total operating current), is grossly rudimentary and highly inadequate to handle the sophisticated and different SEL current profiles arising from various COTS ICs in modern satellites. ZES' LDAP (Figure A1) solution offers a very unique SEL detection and protection by means of intelligently monitoring the unique signature of the SEL current for **virtually all COTS ICs**. Specifically, ZES's LDAP has been demonstrated its efficacy to be able to detect every SEL occurrence and protect the COTS IC (analog, digital and mixed-signal ICs) and without false triggering under irradiation tests, including laser (Figure A2) and in a cyclotron (Figure A3) at Texas A&M University.

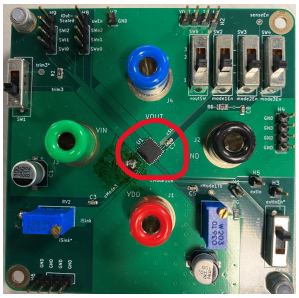


Figure A1 LDAP Evaluation board

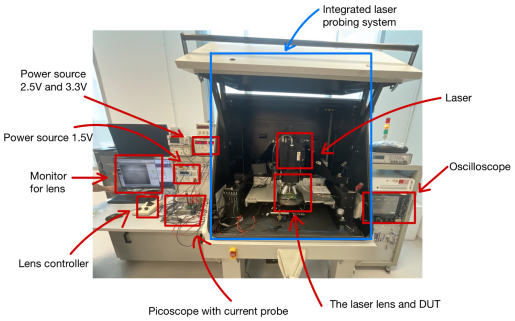


Figure A2 Laser Tests

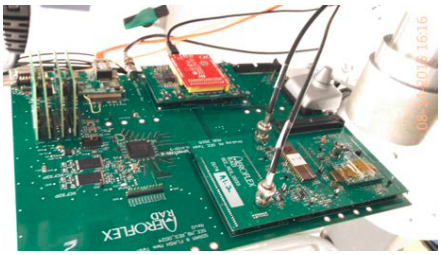


Figure A3 Cyclotron Tests

ZES LDAP Solution

Figure A4 depicts the exemplar diagram of LDAP-protected COTS FPGA. Generally, any powerline that is greater than 1V is likely sensitive to SEL. Hence, it is advisable to protect both 1.5V and 3.3V powerlines if the SEL performance of the COTS FPGA is unknown.

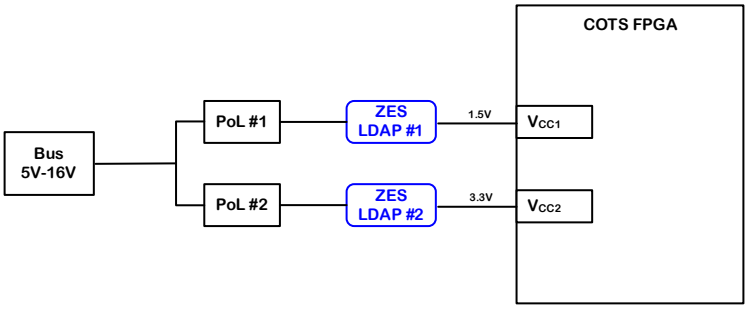


Figure A4 Exemplar Diagram of LDAP-Protected COTS FPGA

However, as the number of powerlines increases, the overheads due to the implementation of ZES LDAP become excessive and unacceptable. In view of this, ZES provides a one-stop turnkey solution that involves the following steps:

(i) Performing a laser test to understand the SEL behavior of the COTS ICs. It is likely that not every powerline is vulnerable to SEL – generally, the powerline with a lower voltage is less sensitive to SEL. As an example in Figure A4, assuming that the laser test shows that the 1.5V powerline exhibits no SEL, only one LDAP is required to protect the 3.3V powerline. In short, the outcome of this laser test is very useful as it allows targeted SEL protection without excessive overheads.

(ii) Following (i), the laser test further evaluates if there is any observation that the driving current from I/Os of the COTS IC sustains the SEL – a phenomenon reported in some COTS ICs.

(iii) Subsequent to (ii) and (iii), an optimized solution to protect SEL-sensitive powerline(s) is proposed – an effective SEL protection, low hardware overheads, low PCB footprint and high value-to-cost ratio; see possible solutions in Figure A5. The proposed solution and its effectiveness are then verified and demonstrated under laser.

(iv) In addition to SEL, laser test can also evaluate SET/SEU when needed and the solution to mitigate SET/SEU can be found in Appendix C of ZES' Voter.

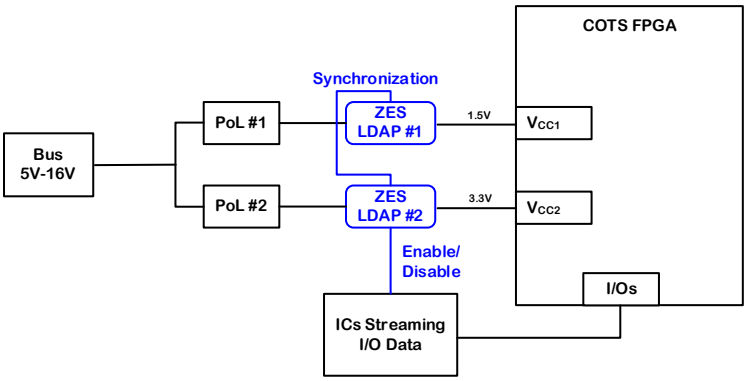


Figure A5 Possible LDAP Solutions: (a) Synchronized LDAPs Protecting Multiple SEL-Sensitive Powerlines and I/Os.

For completeness, ZES is also working on the next generation LDAP solution which would be implemented at the bus to protect entire board, hence offering minimized hardware overheads and cost.

Misconception of the Current Limiter

Although the current limiter has been widely employed in satellites, the reliability of satellites is in fact not improved much in many cases largely because of the common misunderstanding of the role of the current limiter. The current limiter was initially proposed for the purpose of protecting the satellite energy system (i.e. solar panel, battery, power system at satellite bus) from short and overloading faults at satellite subsystems/payloads, and it is now implemented for virtually all satellites.

On the other hand, the SEL protection aims to protect the SEL-sensitive COTS ICs instead, and the SEL behaviour occurring at the semiconductor substrate of these COTS ICs is very different from the aforesaid short and overloading faults at the subsystems/payloads. In view of these, although the current limiter is still being routinely employed for the SEL protection, it is not unexpected that it cannot provide adequate protections for these SEL-sensitive COTS ICs. Specifically, as the current limiter is limited by its operating principle of the overcurrent protection, it is practically impossible for the current limiter to detect SELs in most cases. Figure A6 depicts two examples of misusing the current limiter.

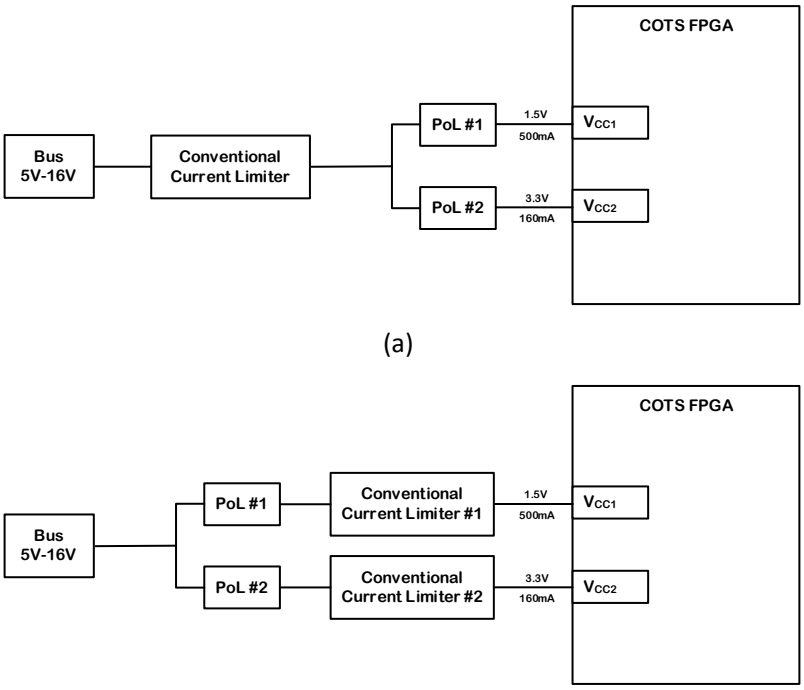


Figure A6 Examples of misuse of the current limiter

Figure A6(a) depicts the misuse of the current limiter at the Bus. As the total operating current can be high and sophisticated at the Bus – the combination of the two nominal currents (500mA from V_{CC1} and 160mA from V_{CC2}) that are distorted by two PoLs respectively, it is virtually impossible for the current limiter to detect any SEL event that only happens at one powerline. For example, consider the induced SEL current at V_{CC2} = 3.3V is 190mA, which is the actual data from the laser test. The combined nominal current at the BUS (5V in this case) is ~260mA, and the current threshold of the current limiter is set at 780mA (typically 3× of the nominal current by accounting for the dynamic current), and the combined nominal current and SEL current is merely 385mA. It is obvious that the current limiter would fail to detect this SEL event at all. For completeness, there is no solution today to detect SELs at the BUS – ZES is in the process of developing this solution. In short, for the purpose of protecting the COTS FPGA from SEL, it is highly recommended not to implement the current limiter at the Bus.

Figure A6(b) depicts the misuse of the current limiter at each individual powerline. Consider the same SEL current at V_{CC2}=3.3V is 190mA and the same nominal current, 500mA from V_{CC1} and 160mA from V_{CC2}. In this case, the current threshold of the current limiter is set at 480mA (typically 3× of the nominal current at V_{CC2} by accounting for the dynamic current), and the combined nominal current and SEL current is merely 350mA. It is also obvious that the current limiter fails again to detect this SEL – the COTS FPGA is damaged during our laser tests because of it. In summary, the current limiter is not an appropriate solution for SEL protections at all.

Demonstration of SEL Protections by ZES' LDAP

ZES' LDAP is designed to provide SEL protections for the individual powerline of COTS ICs. Compared to the current limiter, ZES' LDAP offers several unique advantages and features, and it is best solution for SEL protections. Specifically, as ZES' LDAP monitor the comprehensive current profile instead of the absolute current level by the current limiter, it is able to detect every SEL rapidly.

Figure A7 depicts the waveforms obtained from laser tests, wherein V_{CC2} is sensitive to SEL, and the current at V_{CC2} embodies a complex current profile to emulate low power mode and high power mode, swinging between 20mA and 160mA.

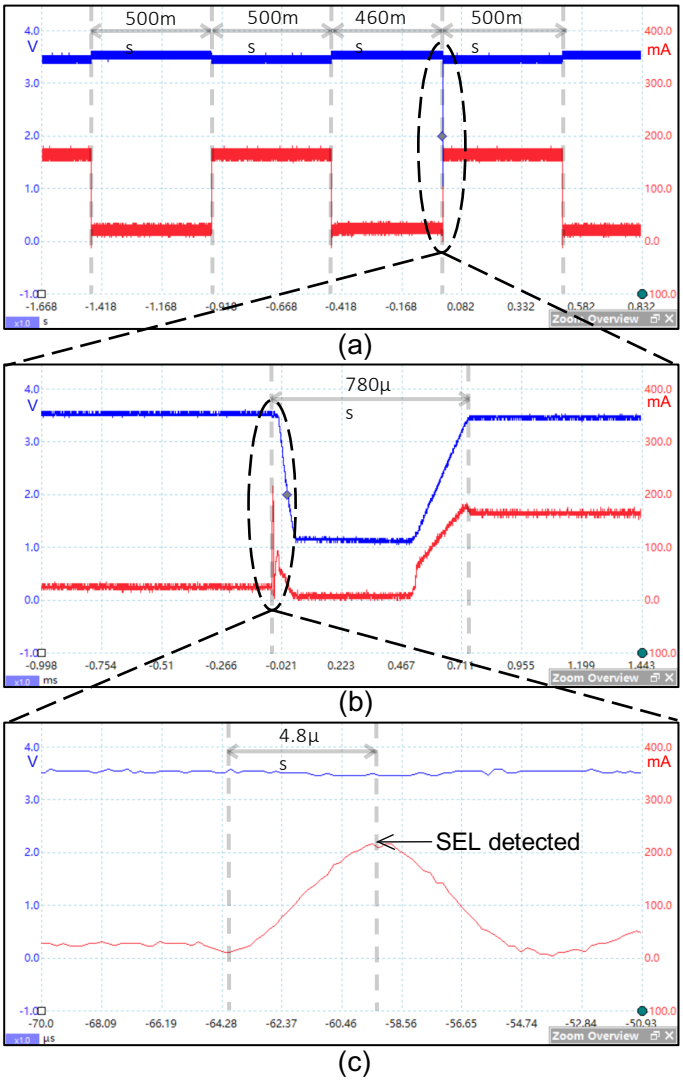


Figure A7 SEL Protections by LDAP under Laser

When the laser scans the SEL-sensitive region of the COTS FPGA, SELs are observed as depicted in Figure A7(c). The current at first jumps from 20mA to 210mA, and subsequently it takes ~4.8µs for LDAP to detect this SEL; once an SEL is detected, the current into the FPGA is immediately cut off and decreases to zero. This observation shows that LDAP correctly and rapidly identifies the SEL current profile from the complex operating current, and successfully removes the SEL current. Figure A7(b) shows that after the SEL current is removed, LDAP takes 780µs (pre-programmed) to keep the power line down and then restore V_{CC2} to 3.3V.

More than 50 SEL events are induced by laser, and ZES' LDAP successfully detects every SEL without any exception. Subsequent to this, the COTS FPGA still functions well. On the other hand, as delineated above, the current limiter indeed fails to detect SELs in this experiment when the current threshold is set to 480mA (3× of the maximum nominal current), and the COTS FPGA with the current limiter is partially

damaged after a few rounds of laser scans. Although it is possible to lower the current threshold of the current limiter to detect the SEL, it is not acceptable in practice as the current threshold is too close to the nominal current, hence subjective to false triggering. For completeness, ZES' LDAP doesn't exhibit any false triggering even with the complex operating current profile.

Alternative method to emulate the SEL event in lab is to

Summary

In summary, ZES' LDAP provides an excellent SEL protection of the COTS FPGA, and the experiment demonstrates that the lifetime of the COTS FPGA protected by ZES' LDAP is substantially enhanced from that with the current limiter.

Point of Load (PoL) in details

Radiation Hardened PoL: ZES's Point-of-Load (PoL) Solution – Radiation-Hardened DC Power Source with Innate Redundancy

The importance of power systems in a satellite cannot be over-emphasized as the majority of satellite mission failures are attributed to the failure of its power system.

PoL Requirements in Space

The DC power source is one of the fundamental building blocks in a satellite power system. In view of modern satellites' comprehensive missions, it is imperative that radiation-hardened PoLs be employed as part of its power system, and if possible, with hardware redundancy. Further, in view of the complex electronics therein and its resource-constraint (particularly form-factor) construction, the PoL needs to be both flexible and power-efficient.

COTS PoL Inadequacy

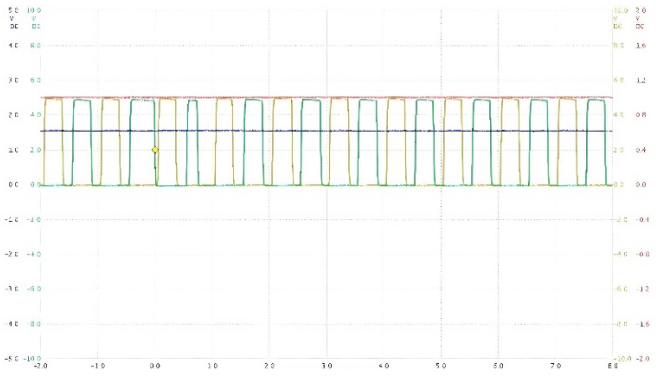
COTS PoLs are generally inadequate in three aspects. First, COTS PoLs are affected by radiation effects, in some cases by Single-Event Latchup (SEL) which is often destructive. Functionally, the operation of COTS PoLs is easily interrupted by Single-Event Transients (SET) which could severely de-stabilize their DC output which in turn disrupt the operation of the electronics powered by the COTS PoL. Second, COTS PoLs require complex and multiple control strategies for better power efficiency over different loading scenarios – this compromises not only the reliability of the COTS PoL DC outputs but also its transient performance. Third, COTS PoLs typically do not allow redundancy. Radiation-hardened PoLs, on the other hand, suffer from the aforesaid second and third shortcomings.

ZES PoL Unique Advantages

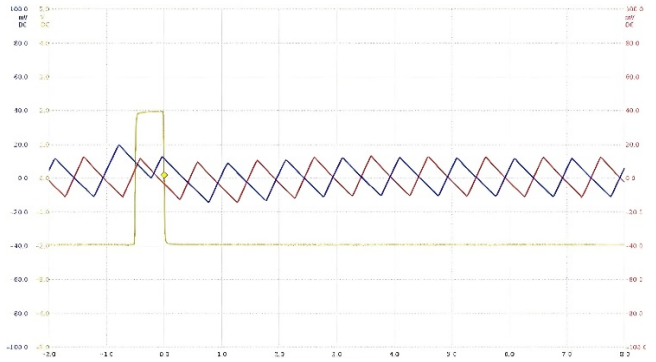
ZES's Radiation Hardened PoL embodies a proprietary (*3 pending patents*) step-down architecture, offering several unique attractive advantages/features over COTS PoLs. First, ZES's PoL **always** operates at its **maximum power efficiency** over a wide loading range, and this is achieved with a unique but simple control strategy. This advantage is highly advantageous to modern satellites in view of their form-factor and limited energy resource. Second, ZES's PoL is radiation-hardened and is inherently insensitive to SEL and SET because its digital-like operation. Third, ZES's PoL innately allows redundancy by paralleling multiple PoLs independently – the **first-ever**. Fourth, ZES's PoL can be realized with very small output inductance, hence substantially small Printed-Circuit-Board footprint, i.e., valuable smaller form-factor. Fifth, ZES's PoL allows high step-down ratio, e.g. 20V-to-1V without compromising any other parameters. When compared to present-day radiation-hardened PoLs, ZES PoL offer the aforesaid first, third, fourth to fifth advantages.

ZES PoL Efficacy in Test

ZES's PoL has been demonstrated its efficacy and advantages under irradiation tests, including laser (Figure A2) and in a cyclotron (Figure A3) at Texas A&M University. Figure B1(a) below depicts the two switching nodes (green and yellow) and the output voltage (blue), and Figure B1(b) depicts two inductor currents (blue and red) and the radiation indicator signal (yellow). It can be observed that when heavy-ion particles hit the ZES's PoL (around 0s in Figure B1(a)), because of ZES's proprietary PoL architecture, two inductor currents compensate each other, hence providing a very clean and stable output voltage.



(a)



(b)

Figure B1 Measured waveforms under irradiations

PoL Design Example

Figure B2 depicts an example of two ZES' PoLs to drive 2 powerlines of the COTS FPGA. ZES' PoL is designed and optimized for the operation with 1A output current and below, hence offering several unique benefits:

(1) The power efficiency of ZES' PoL is optimized for all current below 1A – the power efficiency only decreases slightly when the output current decreases; in contrary, the power efficiency of state-of-the-art rad-hard PoLs degrade severely.
(2) The overcurrent protection of ZES' PoL is tailored for low output current, and can be adjusted.
(3) When higher output current is required, multiple ZES' PoLs can be implemented in parallel. At low output current, only one ZES' PoL outputs current, and when the load demands higher current, other ZES's PoL(s) is activated to output current. In this manner, ZES' PoL always operates at the optimized condition, and also provide innate redundancy.
(4) ZES' PoL is designed to be hardening toward radiations. Based on the heavy-ion tests, its output voltage is virtually unaffected by radiations.
(5) ZES' PoL can employ very small inductor (e.g. 220nH), hence substantially reducing PCB footprint.

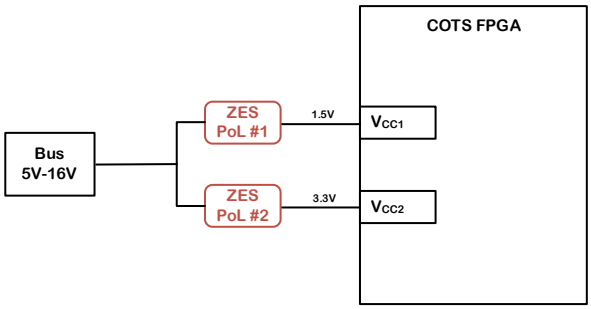


Figure B2 Example of ZES PoL for the COTS FPGA

VOTER for Data Integrity in Details

Radiation Hardened Voter: ZES' Voter – Improving Data Integrity of Commercial-Off-The-Shelf (COTS) in Satellites

It is well known that COTS devices are sensitive to various radiation effects in space, in particular in deep space. Amongst the various radiation effects, Single-Event-Upset (SEU) and Single-Event-Transient (SET) often cause erroneous digital data largely because the data bits are corrupted (from logic '1' to logic '0' or vice- versa) in sequential logic and memories.

To mitigate the corruption of digital data, the common practice to enable COTS devices to be more resilient is to include redundancy, typically by physical redundancy at the cost of hardware overheads. To enable an effective hardware redundancy, the critical assumption is that the voter circuit (serving as a judge to check the outputs of redundancy) must feature an ultra-low error-rate.

Triple Mode Redundancy (TMR)

ZES' voter is designed to support a triple-modular-redundancy (TMR) architecture to accept multiple outputs from COTS devices. ZES' voter is capable of filtering erroneous outputs and/or possibly correcting erroneous outputs of the COTS devices. One ZES' voter has four voting channels (see Fig. C1), allowing to vote up to 4 data bits. For any voting channel where i = 1 to 4, it accepts three input (i.e., A_i, B_i, C_i) and produces a voted output (Y_i) and the error flag (E_i). The voter output (Y_i) follows the majority of the three inputs, and the error flag (E_i) will become logic '1' if at least one input is different from the other two inputs. Fig. C2 depicts the Truth Table of one voting channel. ZES' voter is best applied to the circuit modules for communication protocols, including UART, SPI and I^{2}C. Fig. C3 depicts the demo board showing the error-free UART, SPI and I^{2}C protocols by using ZES' voters.

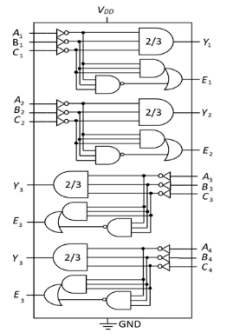


Fig. C1: One ZES' voter having 4 voting circuits

Inputs			Output	
A_i	B_i	C_i	Y_i	E_i
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	1
1	0	0	0	1
1	0	1	1	1
1	1	0	1	1
1	1	1	1	0

Fig. C2: Truth Table for one voting circuit (i = 1 to 4)

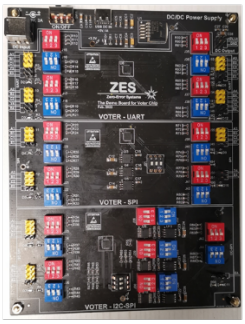


Fig. C3: Demo Board showing the error-free UART, SPI and I^{2}C protocols

VOTER Design Concept

Fig. C4 and Fig. C5 depict a simple design concept how to enable a TMR implementation at the slave interface side of the UART and SPI respectively. Various combinations for realizing TMR at the master and/or slave interfaces can be constructed accordingly.

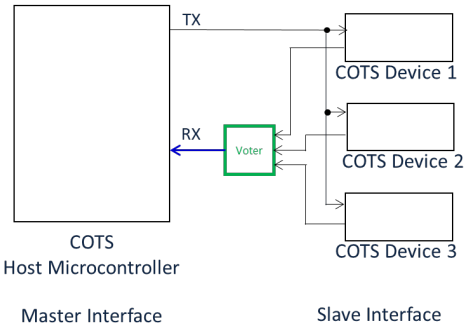


Fig. C4: An UART interface using Voter

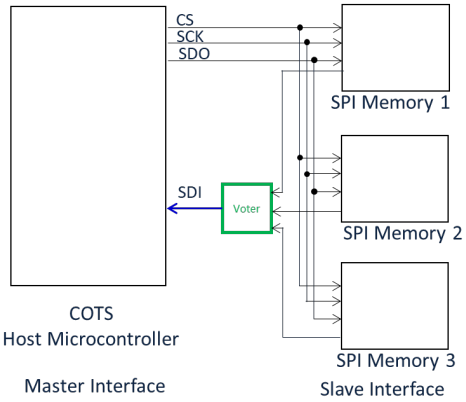


Fig. C5: A SPI interface using Voter

ZES' voter is realized based on ZES's digital Radiation-Hardened-By-Design (RHBD) technologies (patents pending). At this juncture, Laser Testing has been conducted on ZES's voter where there is no SET and Single-Event-Latchup observed with a very high laser energy (up to 6A laser current).