Voter Application Note

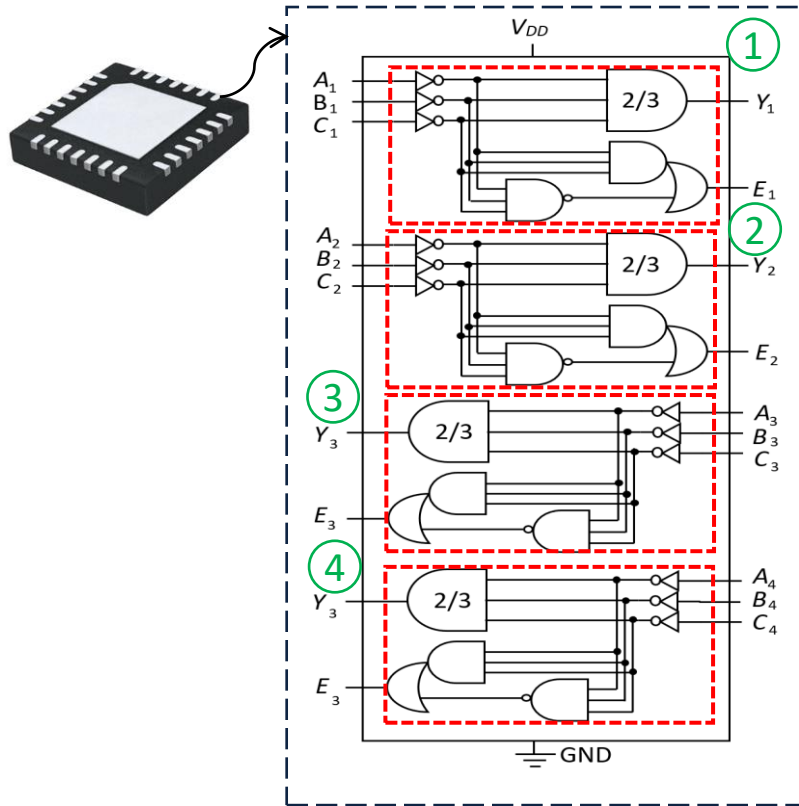Internal Info

Vote Application Note – Basic Info

Fig. 1: One QFN28 voter chip having four independent
voting circuits. Each voting circuit enables
Triple Modular Redundancy (TMR)

Table 1: Truth table for each voting circuit

Input			Output	
A_i	B_i	C_i	Y_i	E_i
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	1
1	0	0	0	1
1	0	1	1	1
1	1	0	1	1
1	1	1	1	0

Voted output – Majority wins
based on 3 inputs
(for data integrity)

Error flag – At least one input
is different
(for error detection)

Voter Application Note – Data Integrity for Interfaces

Added Part(s)

Voter

COTS Device

COTS Device

COTS Device

COTS Microcontroller

COTS Device

COTS Microcontroller

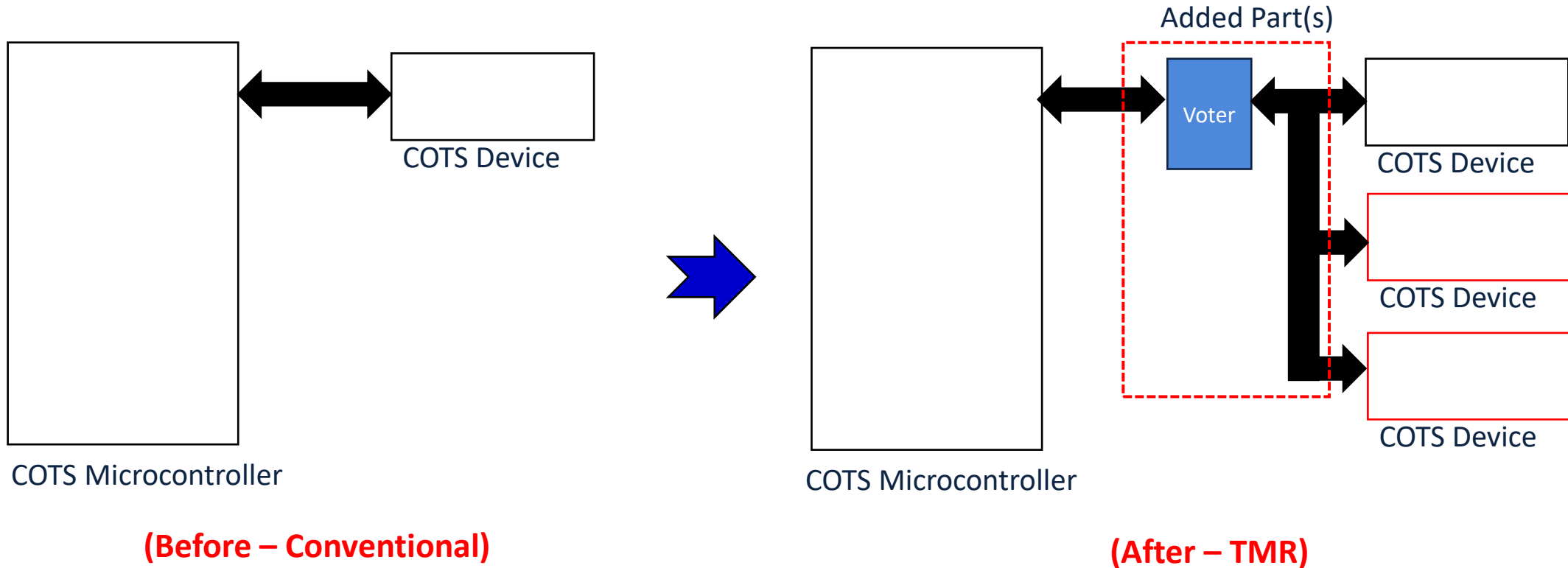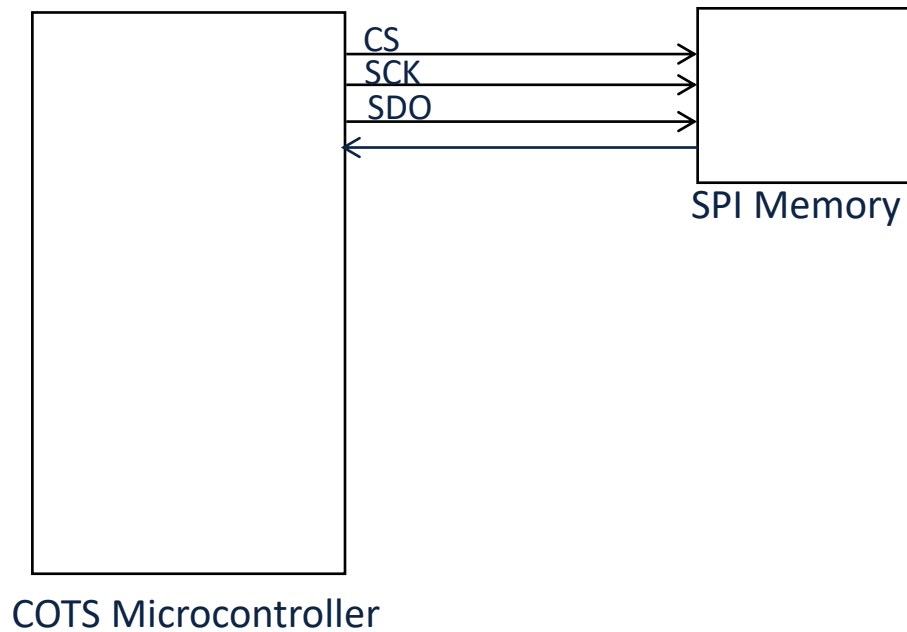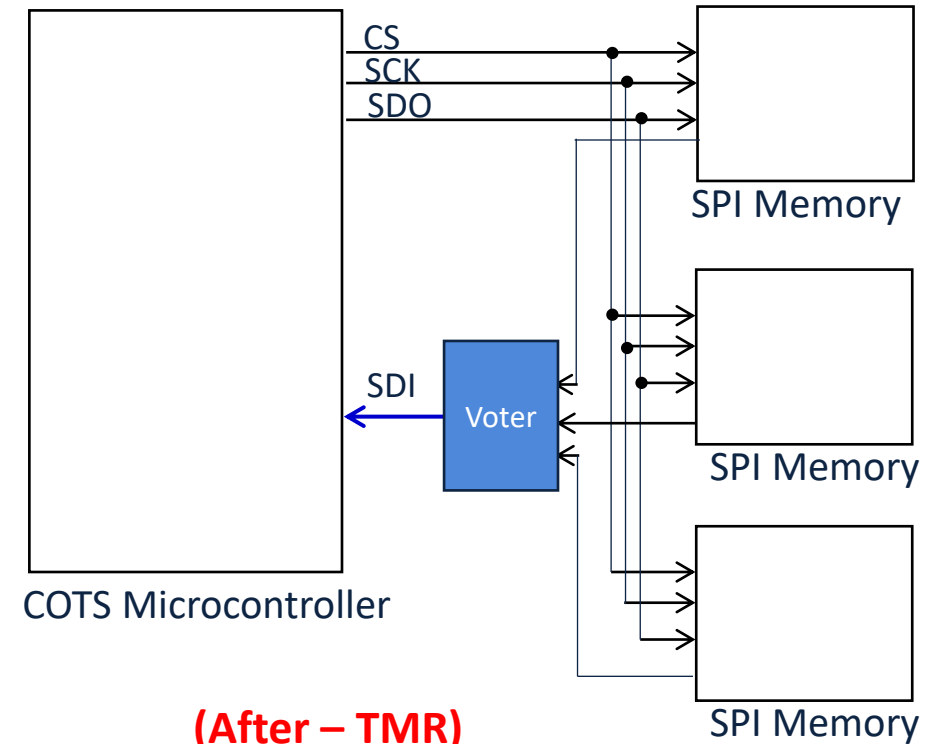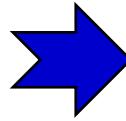**(Before – Conventional)**

(After – TMR)

Fig. 2A: Original setup (without hardware data integrity protection)

Fig. 2B: Modified setup (with hardware data integrity protection) – There is no need to modify the interface protocols or firmware. Tested interface protocols include UART, SPI, I^{2}C.

Voter Application Note – Example: SPI Memory Interface
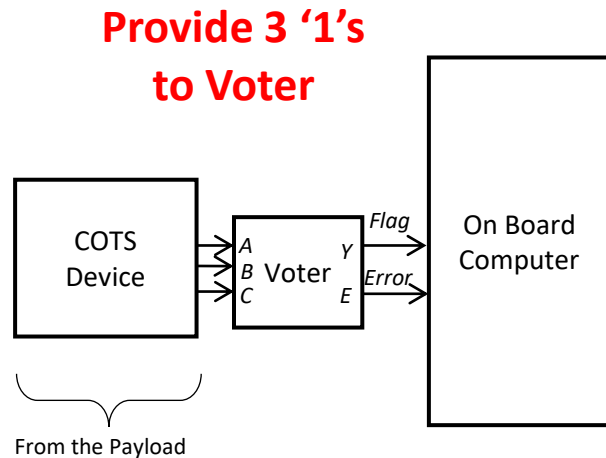

Fig. 3A: Original setup for an SPI Interface

Fig. 3B: Modified setup for a TMR SPI Interface

Voter Application Note – Example: Watch Dog Signal

Provide 3 '1's to Voter

Input			Output		Meaning
A	B	C	Flag	Error	
0	0	0	0	0	Chip may be damaged
0	0	1	0	1	Chip has SEUs, caution
0	1	0	0	1	
0	1	1	1	1	
1	0	0	0	1	
1	0	1	1	1	
1	1	0	1	1	
1	1	1	1	0	Chip Healthy

Voter Application Note – Design Concept for TMR

TMR can be applied at the Master side (e.g., Sub-System A) or at the Slave side (e.g., Sub-System B) or at both sides
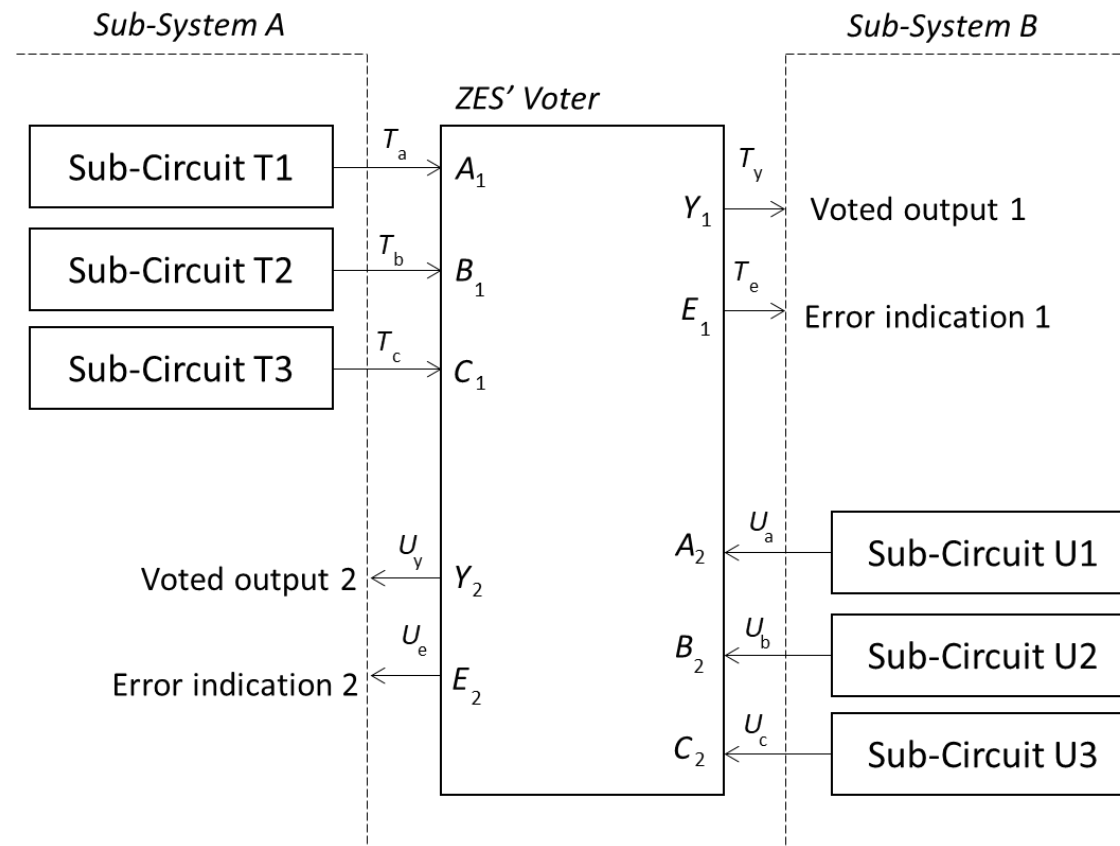

Fig. 4: General Setup concept for TMR embodying Voter

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End of Presentation
--- Thank You ---

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