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ZES
ZERO-ERROR SYSTEMS

Draft Rev 1.9/ October 2024

ZES100 - Latchup Detection and Protection (LDAP)

Enabling Advanced Commercial-Off-The-Shelf (COTS) to 'Space-Grade'

Description

ZES100 is an integrated solution designed to detect Single-Event Latchup (SEL) in a target device and subsequently provide a recovery. It can be used to protect power supply and Commercial-Off-The-Shelf (COTS) devices from anomalous current due to SEL.

ZES100 is based on ZES's proprietary technology, offering an unprecedented means to protect COTS from SEL – enabling advanced COTS devices to space. Specifically, ZES100 incorporates two levels of protections. First, ZES100 can detect the early onset of SEL occurrence, including micro-SEL, a localized SEL whose current is often relatively low. Second, ZES100 can also provide an overall current limit. Collectively, two levels of protection efficiently remove SEL by an appropriate power cycling.

ZES100 is immune to Single-Event Transient (SET) and Single-Event Upset (SEU), and is unaffected by long-term drift current due to Total Ionized Dose (TID).

Internal power switch with Low on-resistance (R_{DSONP}) of 10mohm at Vgs =-4.5V with 500mA.

High integration makes ZES100 an ideal candidate to protect advanced COTS devices in space.

Applications

- Space and Industrial application.
- Satellite and Payload power management control and distribution.
- Application for aircraft and automotive available.

Features

- Fast response to SEL
- Detection of the SEL occurrence at on-set
- Detection of micro-SEL
- Automatic and adjustable power cycling
- Immune from current drift due to aging and TID
- Wide-range supply voltage and loading current
- Space qualified technology
- Radiation Hardened by Design (RHBD)
- Qualified for space enhanced plastic (SEP)
- ITAR free
- Over current short protection
- Evaluation Kit available

Electrical Performance

Input Voltage	1.2V-5V
Continuous Loading Current	1mA-500mA*
Power Cycling Time	Adjustable
Operating Temperature	-55°C to 125°C
Voltage Drop	0.1V @ 500mA, 5V

Radiation Performance (Cyclotron Verified)

TID	300 Krad (Si)
SEL	110 MeV-cm^2/mg
SEFI	110 MeV-cm^2/mg
SEU	110 MeV-cm^2/mg
Ion Fluence	Up to 10^7/cm^2

Ordering Information

Part No.	Grade	Form Factor	Size
ZES100LDPFQ-EP	Space Plastic Flight Model	QFN32L	5 mm × 5 mm
ZES100LDPGQ-EP	Space Plastic Ground Model†	QFN32L	5 mm × 5 mm
ZES100LDPGEV-EP	Evaluation Module†	PCBA	80 mm x 80 mm

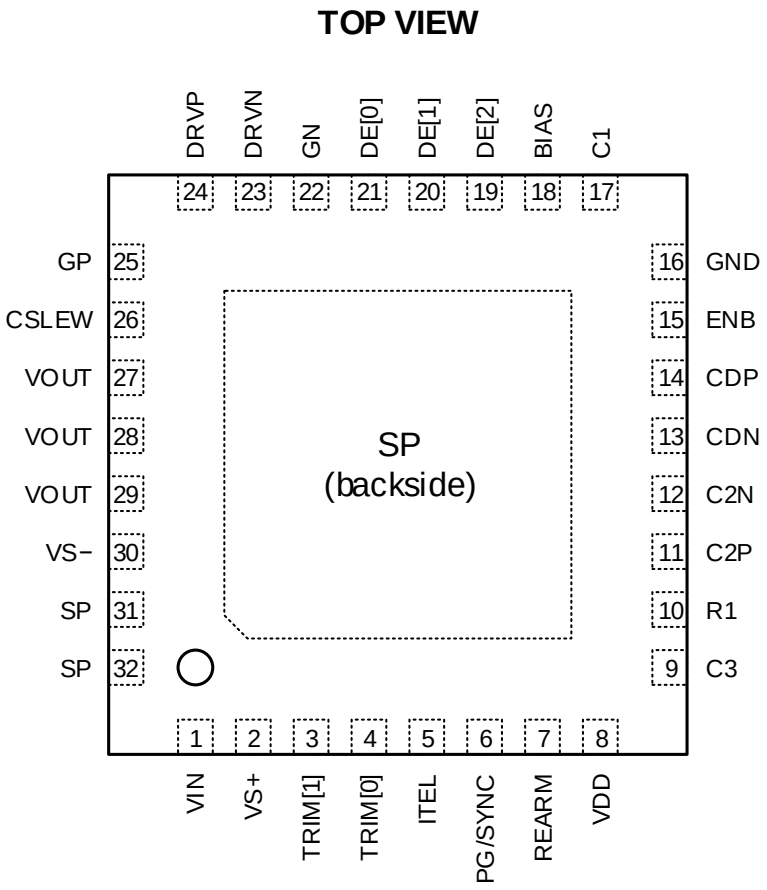
For price, delivery, and ordering information please contact info@zero-errorsystems.com.

* Higher current can be achieved if an external switch is employed.

† These units are intended for engineering evaluation only. These units are not suitable for qualification, production, radiation testing or flight use. Parts are only tested in room temperature, and hence not warranted for performance over the full specified temperature range of –55°C to 125°C or operating life.

1 Pin Configuration

1.1 ZES100 Pin Connections (QFN32: 5mm x 5mm)



US Patent No.: 10,566,780 B2

1.2 Pin Description

Table 1 ZES100 Pin Description

*In – input, Out – Output

Pin	In/Out*	Name	Description
1	In	V_{IN}	**Input voltage**.
2	In	V_{S+}	**Current sensing** pin. Connect a resistor R_{SEN+} to this pin and V_{IN}.
3, 4	In	TRIM[1:0]	Input **Trimming bit** to determine SEL detection rate.
5	Out	I_{TEL}	**Telemetry** output proportional to sensed current. Connect a resistor to this pin and V_{DD}.
6	Out / In	PG/SYNC	**Power Good/Synchronize** pin Connect a resistor to this pin and V_{DD} (required). An open-drain input-output that goes low if V_{OUT} is outside a specified regulation window, i.e. a power-good PG. It can be also used as a synchronization input to synchronize the power shutdown of multiple devices.
7	In	REARM	Use during Power recycle/recovery, connect a capacitor to this pin and GND to set the delay before rearming detection.
8	In	V_{DD}	**Supply** of ZES100.
9	In	C3	Connect a capacitor to this pin and V_{DD}.
10	In	R1	Connect a resistor to this pin and V_{DD} to set **max current threshold**.
11, 12	NA	C2P, C2N	Not connected
13, 14	In	CDN, CDP	Connect a capacitor to these pins to set the **power-cycle duration**.
15	In	ENB	***Enable pin** (active low) of the DRVP and DRVN pins. When ENB = "0", the internal circuitry controls the DRVP and DRVN pins. When ENB = "1", DRVP = V_{DD}, DRVN = V_{DD}. (switch off)
16	NA	GND	**Ground**.
17	In	C1	Connect a capacitor to this pin and GND to set the **blank period** of overcurrent event.
18	Out	BIAS	**Bias current**, connect a resistor to this pin and GND.
19 - 21	In	DE[2:0]	**Detection Enable** input pins.
22	In	GN	**Gate** pin of internal power **NFET**.
23	Out	DRVN	**NFET driver** output.
24	Out	DRVP	**PFET driver** output.
25	In	GP	**Gate** pin of internal power **PFET**.
26	In	C_{SLEW}	Connect a capacitor to this pin and to set the **slew rate of V_{OUT}** when the power transistor is switched on.
27 - 29	Out	V_{OUT}	**Output** of power switch.
30	In	V_{S-}	**Current sensing** pin. Connect a resistor R_{SEN-} to this pin and V_{IN}. It is recommended to connect V_{S-} and SP only at the R_{SEN-} pin.
31, 32 and EP	In	SP	**Source of power** PFET. Connect a resistor R_{SEN-} to this pin and V_{IN}. It is recommended to connect V_{S-} and SP only at the R_{SEN-} pin.

***ENB pin (active low), when ENB=”0” means 0V(GND) and when ENB =”1” means V_{DD}.

2 Typical Application Diagram

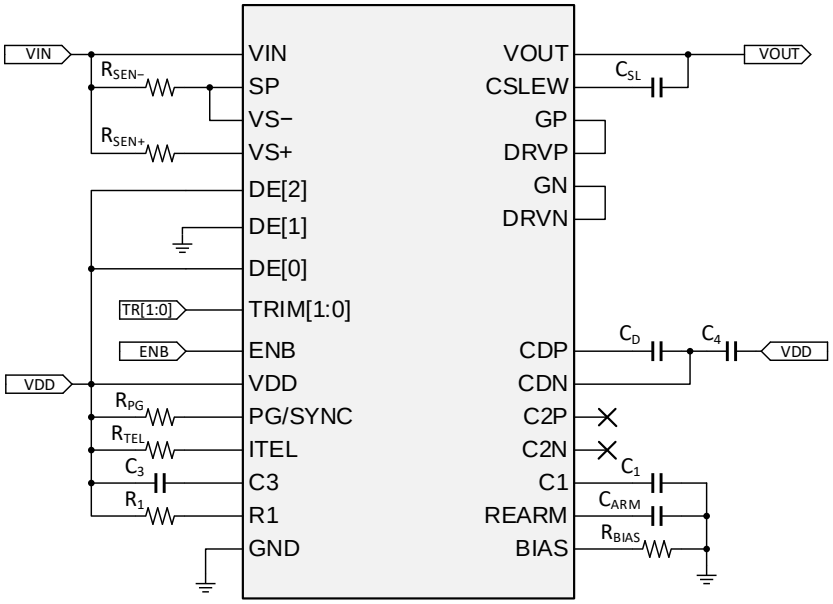


Figure 1 Typical application circuit

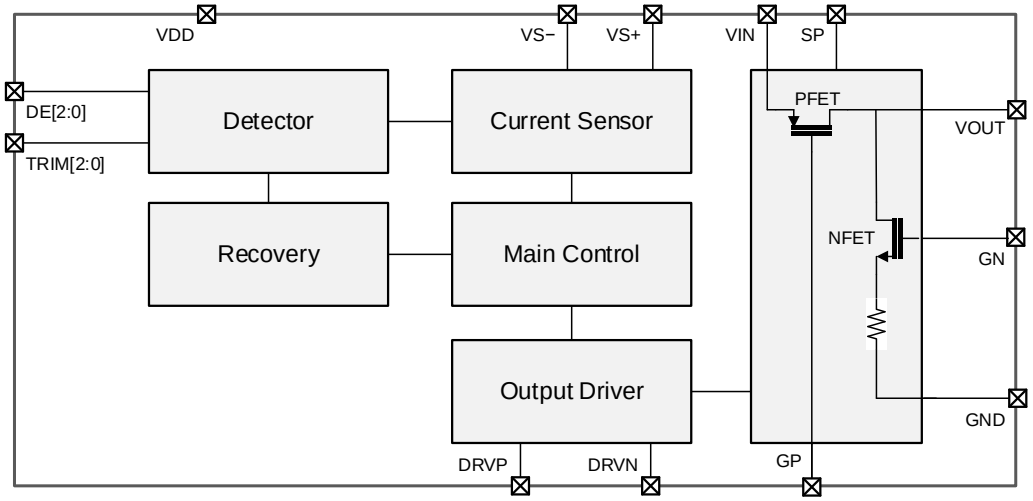


Figure 2 Simplified block diagram

3 Maximum Ratings

Absolute maximum ratings are limits beyond which damage to the device may occur. Exposure to absolute rating conditions for extended periods may affect device reliability. Functional operation of the device at these conditions is not implied.

Table 2 Absolute maximum ratings

Parameter	Min	Max	Unit
V_{IN} Voltage	−0.3	5.5	V
V_{OUT} Voltage	−0.3	5.5	V
V_{DD} Voltage	−0.3	5.5	V
DE[2:0], TRIM[1:0] Voltages	−0.3	5.5	V
PG/SYNC Voltage	−0.3	5.5	V
ENB Voltage	−0.3	5.5	V
SP Voltage	−0.3	5.5	V
C_{SLEW} Voltage	−0.3	5.5	V
REARM Voltage	−0.3	5.5	V
R1, BIAS Voltages	−0.3	5.5	V
C1, C2P, C2N, C3, CDP, CDN, C4 Voltages	−0.3	5.5	V
DRVP, DRVN Voltages	−0.3	5.5	V
GP, GN Voltages	−0.3	5.5	V
V_{S+}, V_{S-} Voltages	−0.3	5.5	V
I_{TEL} Voltage	−0.3	5.5	V
Maximum continuous switch current I_{max}		1	A
Maximum pulsed switch current I_{pulse}		1.4	A
I_{TEL} Current	0	2	mA
I_{BIAS} Current	0	100	µA
ESD Susceptibility (Human Body Model)	-	+/-2000	V
Maximum junction temperature, T_j	-55	+150	°C
Soldering Temperature recommendation		+260	°C
Storage temperature T_{STG}	−55	+150	°C

*Maximum pulsed switch current is RMS value tested with repetitive sine pulse.

4 Electrical Characteristics

Typical values correspond to T_J = 25˚C. V_{IN} = V_{DD} = 5V unless otherwise specified.

Table 3 Electrical Characteristic

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Supply Specifications						
V_{IN}‡	Input voltage		1.2	5.0	V_{DD}	V
I_{IN}	Input Current		1		500	mA
V_{DD}	Voltage Supply of ZES100		2.5	5.0	5.0	V
I_{DD}	Input Current for ZES100	V_{DD} = 5V		10		mA
I_{BIAS}	Bias Current			50	60	µA
Input Specifications						
TRIM[1:0]$_{(th)}$	TRIM[1:0] Threshold			0.5V_{DD}		V
DE[2:0]$_{(th)}$	DE[2:0] Threshold			0.5V_{DD}		V
ENB$_{(th)}$	ENB Threshold	Enable ("0")	0		0.5	V
		Disable ("1")	V_{DD}-0.5		V_{DD}	V
Output Specifications						
V_{OUT}	Output Voltage				V_{IN}	V
I_{OUT}	Output Current		1		500	mA
$V_{GS(th)}$	Gate-Source Threshold Voltage	V_{DS} = V_{GS}, I_D = -300uA			-1	V
I_{GSS}	Gate-Source Leakage	V_{DS} = 0V, V_{GS} = -5V			5	uA
I_{SB}	Standby current	ENB = 5V, V_{OUT} = 0V			4	uA
I_Q	Quiescent current	ENB = 0V, V_{IN} = 0V = V_{OUT}	2.6	3.8	5	mA
t_{ON}	Turn on time	ENB = 0V, R_L=10ohm, C_L = 10uF			200	us
t_{OFF}	Turn off time	ENB = 5V , R_L=10ohm, C_L = 10uF			60	us
R_{DSONP}	Power PFET R_{DSON}			10		mΩ
Detection						
I_{TH}	Max Current Threshold	R_1 = 10.5kΩ		500		mA
T_{BLANK}	Blank Period	C_1 = 10nF		0.24		ms
Timing						
T_{CYCLE}	Power-Cycle Duration	C_D = 10nF		0.6		ms
SLR	Slew Rate of V_{OUT}	C_{SLEW} = 10nF		16.2		V/ms
Telemetry						
PG/SYNC	Power-Good/Sync Voltage	R_{PG} = 100kΩ	0		V_{DD}+0.3	V
I_{TEL}	Telemetry Voltage	R_{TEL} = 1.5kΩ	0.6		V_{DD}+0.3	V

‡ V_{IN} must be always equal to or lower than V_{DD} at any time.

US Patent No.: 10,566,780 B2

5 Device Description and Operation

5.1 Overview

The ZES100 is a versatile monolithic device designed for satellite applications to provide protection on both power supply and COTS devices in case of anomalous current demand due to SEL. This device can be configured to detect SEL and micro-SELs using ZES's proprietary technology, in addition to the basic current limiter function. With both detection mechanisms, power supplies which work in harsh radiation environment are protected from damage caused by SELs.

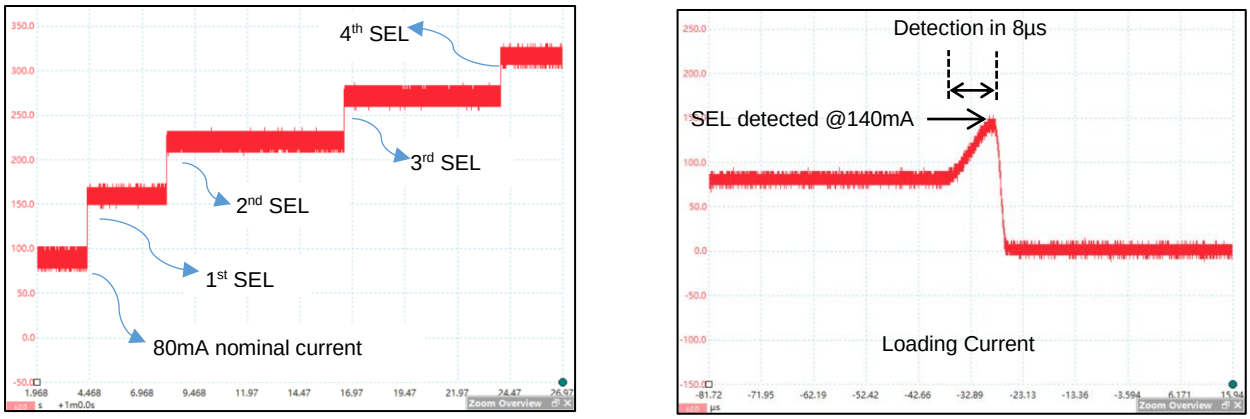


Figure 3 Demonstrations of accumulated micro-SELs induced by Laser

The power supply bus V_{IN}, under ZES100 protection, has a voltage ranging from 1.2V to V_{DD} where V_{DD} ranging from 2.5V to 5V. When a device under protection (DUP) requires multiple supply voltage domains, multiple ZES100 devices can be configured to allow synchronized power cycling when one of the voltage domains is affected by SEL.

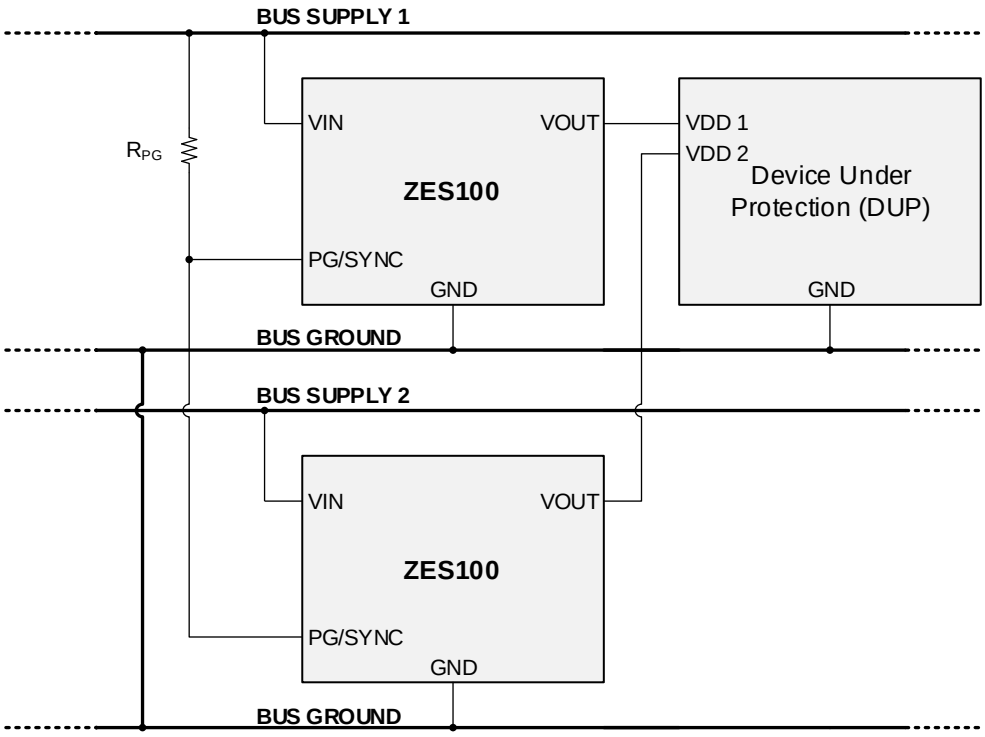


Figure 4 Multiple Supplies synchronized power cycling configuration

The core of the device consists of current sensing, latchup detection, recovery, and telemetry functions designed for high reliability system implementation.

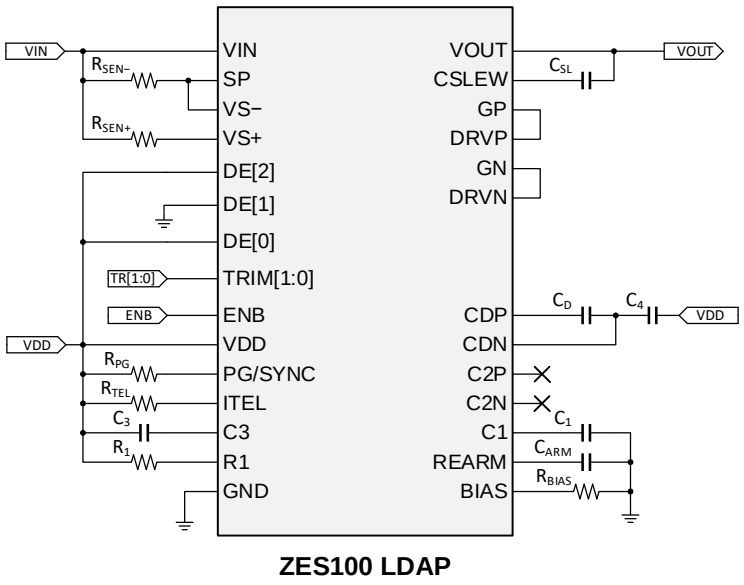


Figure 5 Typical application circuit implementation

Table 4 Typical values of implementation for current limit of ~500mA, current ratio of ~340

Symbol	Typical Value	Unit
R_{SEN-}	15 ±1%	mΩ
R_{SEN+}	5.1 ±1%	Ω
R_{PG}	100	kΩ
R_{TEL}	1 ±1%	kΩ
R_1	18 ±1%	kΩ
R_{BIAS}	470 ±1%	Ω
C_1	10 ±5%	nF
C_3	10 ±5%	nF
C_4	10 ±5%	nF
C_D	10 ±5%	nF
C_{SL}	10 ±5%	nF
C_{ARM}	1 ±5%	nF

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5.2 Current Sensing

ZES100 has a built-in current sensor to read the current through V_{OUT}, i.e., the output/load current I_{OUT} as the sensed current I_{SEN} with a certain current sensing ratio. The current sensing ratio between I_{OUT} and I_{SEN} can be customized using R_{SEN-} and R_{SEN+} resistors by the following relationship.

$$r = \frac{I_{OUT}}{I_{SEN}} = \frac{I_{OUT,MAX}}{I_{SEN,MAX}} = \frac{R_{SEN+}}{R_{SEN-}}$$

The current sensing ratio depends on the load and the absolute maximum rating ZES100's internal sense current branch (~2mA). For example, for a Device Under Protection (DUP) with max supply current, $I_{OUT,MAX}$ of 500mA, we can limit the maximum sensed current $I_{SEN,MAX}$ to 1.47mA (additional derating) to obtain current sensing ratio of 340. If the R_{SEN-} resistance is set to be 15mΩ, then the R_{SEN+} resistance is 5.1Ω. It is recommended to design the minimum voltage drop across R_{SEN-} of 5mV with refer to below **Table 5**.

Table 5 Recommended Current Sensing ratio

I_{OUT} (mA)	MOSFET	R_{SEN-} (mΩ)	R_{SEN+} (Ω)	Current sensing ratio, **r**	I_{OUT} x R_{SEN-} (**mV** ≥5mV)	(I_{OUT} x R_{SEN-})/ R_{SEN+} (**mA** <2mA)
1	Internal	15000	10	0.67	15	1.50
5	Internal	3000	10	3.33	15	1.50
10	Internal	1500	10	6.67	15	1.50
50	Internal	300	10	33.33	15	1.50
100	Internal	150	10	66.67	15	1.50
250	Internal	30	5.1	170.00	7.5	1.47
500	**Internal**	**15**	**5.1**	**340.00**	**7.5**	**1.47**
1000	External	8	5.1	637.50	8	1.57
1500	External	10	10	1000.00	15	1.50
2000	External	**15**	**20**	**1333.33**	**30**	**1.50**
5000	External	15	49.9	3326.67	75	1.50
10000	External	8	49.9	6237.50	80	1.60
20000	External	8	100	12500.00	160	1.60

Note: The above $R_{SEN+/-}$ values are for reference only, please check with ZES for verification.

The current sensing ratio accuracy may be affected by several factors such as parasitic resistance of PCB traces, resistors tolerance, internal offset, etc. To mitigate the impact of parasitic resistance of PCB traces, it is recommended that the PCB route from R_{SEN-} to V_{S-} (low current path for sensing) is isolated from the route from R_{SEN-} to SP (high current path). **Figure 6** depicts a PCB layout example where the two paths are only connected together at one of the R_{SEN-} pads such that the voltage sensed by V_{S-} will be less affected by the voltage drop due to parasitic resistance of the PCB trace.

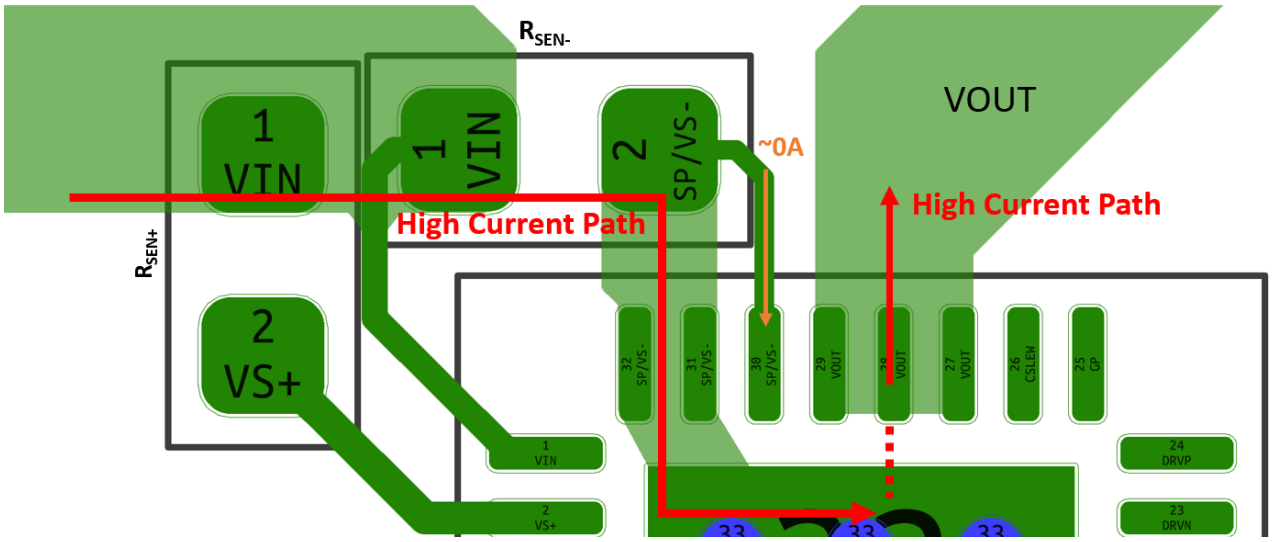


Figure 6 PCB layout recommendation for a better current sensing accuracy

5.3 Latchup Detection

5.3.1 Major-SEL, Micro-SEL and Overcurrent Detection

The ZES100's major-SEL/micro-SEL detections can be activated with detection enable DE[2:0] pins. To maximize the benefits of ZES100, it is highly recommended to set DE[2:0] = '101'.

Figure 7 depicts the V_{OUT} and PG signals during a power cycling when a major-SEL/micro-SEL occurs. The V_{OUT} remains stable after the power cycling as the latter removes the unwanted state. Under general scenarios, a power cycling is appropriate to remove all SELs.

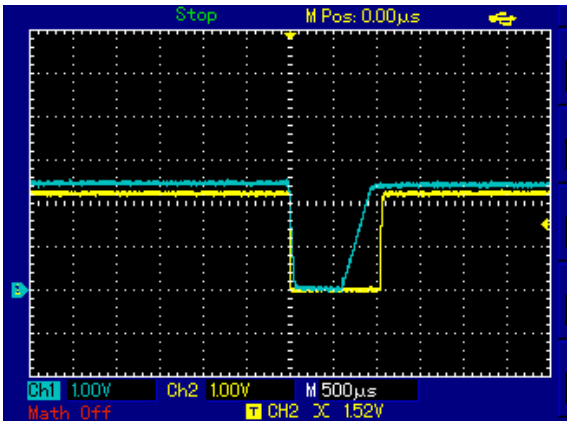


Figure 7 Waveforms of V_{OUT} (blue) and PG (yellow) during a power cycling when an SEL occurs.

The SEL/µSEL detection configuration depends on the TRIM[1:0], and C_3 capacitance. The TRIM[1:0] is a 2-bit (MSB...LSB) signal that set the built-in monotonic threshold levels. A lower TRIM[1:0] value increases the detection sensitivity; typical TRIM[1:0] is set to "00". A higher C_3 also increases the detection sensitivity; typical C_3 is set to 10nF.

ZES100 also operates as a current limiter that detects a general over load current event (e.g. Short circuit at the Load), and subsequently initiates a recovery sequence after a blank period T_{BLANK}. If the Device Under Protection (DUP) remains in the overcurrent state after T_{BLANK}, ZES100 will initiate another recovery sequence that primarily consists of a power cycling.

In a scenario where a power cycling could not remove the overcurrent state, e.g. permanent damage, the power cycling sequence will be repeated until the overcurrent state is removed or the ZES100 is disabled. **Figure 8** depicts the V_{OUT} and PG signals when overcurrent occurs and could not be removed.

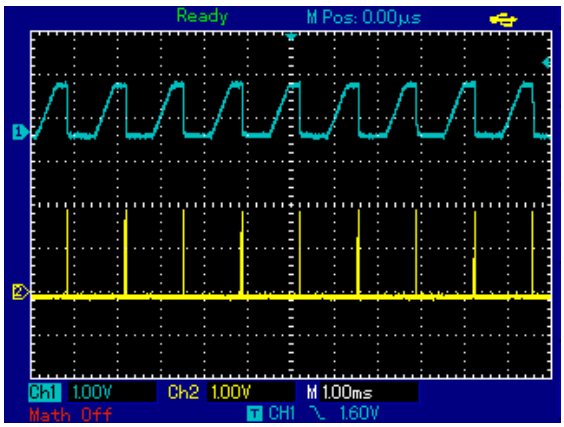


Figure 8 Waveforms of V_{OUT} (blue) and PG (yellow) during power cycling when an overcurrent occurs and sustains after a power cycling.

A. Blank Time

The detection blank time is the duration between the event when an overcurrent is first detected and the recovery action is initiated. It enables additional filtering of unwanted supply current noise or glitches that may cause false detection.

The blank time can be programmed by setting the C_1 value with the following relationship.

$$C_1 \cong \frac{T_{BLANK}(\text{in seconds})}{25000} \quad F \tag{1}$$

5.4 Recovery

ZES100 initiates a recovery sequence when it detects overcurrent/major-SEL/µSEL events. The recovery sequence consists of power cycling, rearm of detection, and V_{OUT} ramp-up control or slew rate.

5.4.1 Power Cycling and Slew Rate Control

The power cycling duration T_{CYCLE} can be broken down into fall, 'off', and rise times as tabulated in **Table 6**.

Table 6 The breakdown of power cycling duration

Time	Dependencies
Fall time	Internal $R_{PULL\text{-}DOWN} \approx 50\Omega$, output capacitor C_{OUT}, and V_{IN}
"Off" time	Delay capacitor C_D
Rise time	Slew rate control, R_{DSONP}, $R_{SEN\text{-}}$, C_{OUT}, and V_{IN}

Depending on the required accuracy of T_{CYC}, users may need to consider the above dependencies. In typical application, the T_{CYC} can be approximated by the "off" time duration by the following equation.

$$T_{CYCLE} \cong T_{OFF} \approx 7 \times 10^4 C_D \tag{2}$$

Additionally, ZES100 can program the V_{OUT} ramp-up rate (slew rate) for devices that require controlled supply voltage ramp-up during start up or power cycling. The V_{OUT} ramp up slew rate can be configured by C_{SL} capacitance and their relationship is approximated by:

$$SR = \frac{dV_{OUT}}{dt} \approx \frac{V_{IN} \times (-0.9)}{2.5 \times 10^4 \times C_{SL}} \quad V/s \tag{3}$$

5.4.2 Rearm of Detection

At the end of power cycling sequence, the inrush supply current of DUP may inadvertently introduce a false detection. The REARM pin can be used to temporarily disable ZES100's detection block when the output is not ready. The rearm of detection will start after a delay T_{REARM} that can be estimated as follows.

$$T_{REARM} \cong C_{ARM} \times \frac{VDD}{2 \times I_{BIAS}} \tag{4}$$

5.5 Synchronization

The ZES100 supports synchronization of multiple ZES100 devices akin to a multi-channel system. In each channel, one ZES100 provides protection to a single supply line or domain. When one of the channels initiates a power cycling sequence, it will trigger power cycling at the other channels. The power cycling duration of each channel is independent of each other.

The synchronization feature can be implemented by simply connecting the SYNC pin (shared with PG) of multiple ZES100 devices to a pull-up resistor R_{PG}. **Figure 9** depicts an example circuit implementation of synchronization of ZES100s to protect a DUP with two supply inputs.

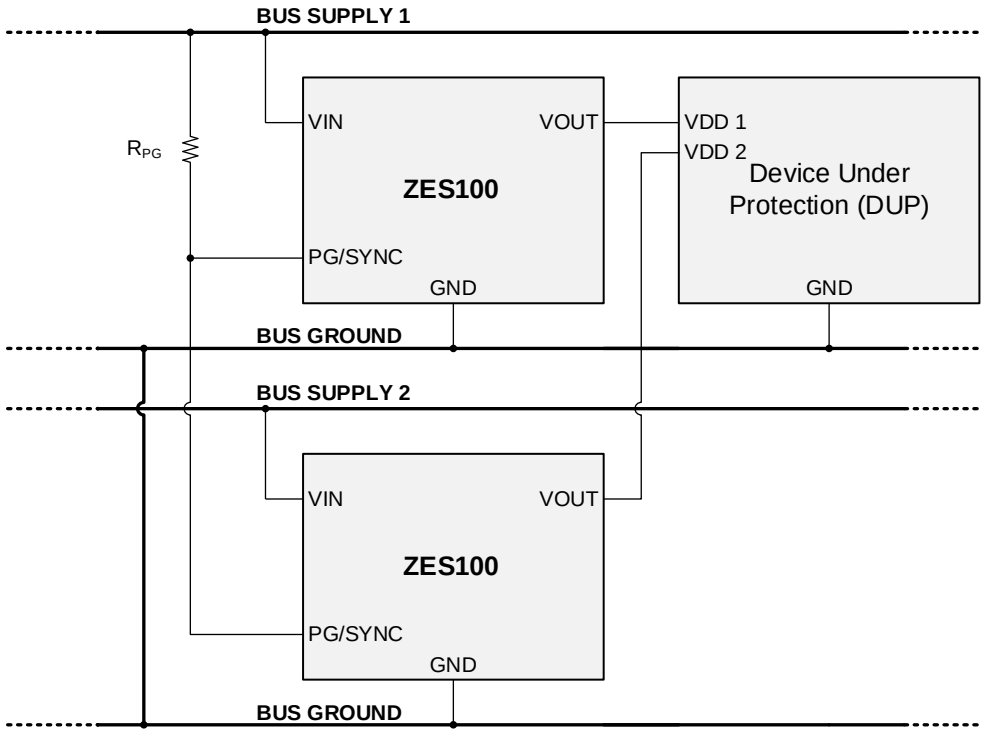


Figure 9 Example circuit of synchronized ZES100s to protect a DUP with two supply inputs

5.6 Status Telemetry

5.6.1 PG (Power Good)

The ZES100 includes an open-drain power good PG pin (shared with SYNC pin) that provides the status of V_{OUT}. PG is '1' when V_{OUT} is approximately >0.9V_{IN}, otherwise PG is '0' or pulled-down. The pull-up R_{PG} value can range 10k-100kΩ.

5.6.2 I_{TEL} (Telemetry)

The telemetry circuit provides information about the load current. The current that flows through I_{TEL} pin is proportional to the current flowing from the bus supply line to the load. The voltage V_{RTEL} across an external resistor R_{TEL} that is connected between V_{DD} and I_{TEL}, is proportional to load current.

The relationship between V_{RTEL} and load current is as follows.

$$V_{RTEL} = VDD - R_{TEL}\left(\frac{I_{OUT}}{r} + 2 \text{ x } I_{BIAS}\right)$$

Where r is the current sensing ratio, and
I_{BIAS} is the current through BIAS pin. (5)

5.7 Enable Pin (ENB)

The ZES100 includes an enable ENB pin (active low) to indirectly control the power switches through DRVP and DRVN pins. **Table 7** tabulates the truth table of ENB pin. By setting ENB to "1", the power switches can be switched off.

Table 7 Truth table of EN

EN	Behavior
0	Normal operation, DRVP and DRVN outputs depend on ZES100's control
1	DRVP = V_{DD}, DRVN = V_{DD} (switch off)

5.8 External Power Switches (for higher I_{OUT})

The ZES100 has a built-in power PFET switch, and a pull-down NFET switch (in series with a 50 Ω resistor). Both the built-in switches are de-rated and their gates are accessible through GP and GN, respectively. The max drain-source current of the power PFET is 500mA at 125°C. These power switches can be driven by ZES100's drivers DRVP and DRVN. To use the built-in power switches, simply connect DRVP to GP, and DRVN to GN as depicted in **Figure 5**.

The ZES100 also supports the use of an external power switch (P-type) to deliver higher $\mathbf{I_{OUT}}$ to load. **Figure 10** depicts an example circuit configuration to implement ZES100 with an external power transistor.

*Recommendation for the selection of external switch, the Gate-Source Threshold Voltage $V_{gs(th)} > V_{IN} – 0.2V$.

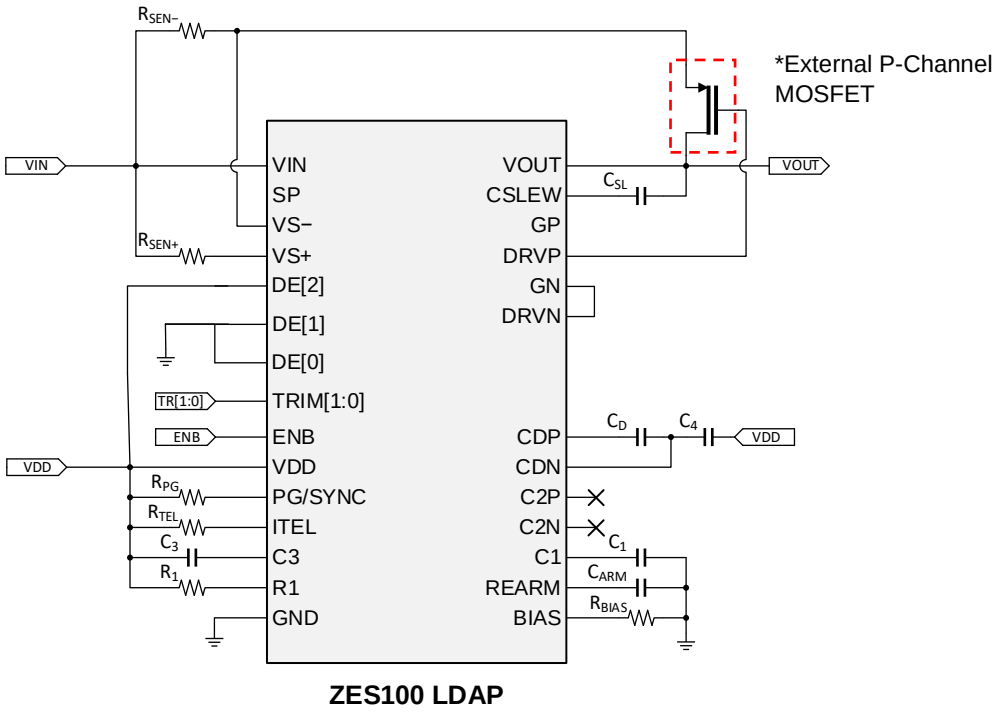


Figure 10 Example circuit configuration to implement ZES100 with an external power switch.

(1)

6 Design Recommendations

6.1 Input and Output Capacitors

Integration of ZES100 into a system requires some considerations in the selection of both input capacitor C_{IN} and output capacitor C_{OUT} as these capacitors could induce sensitivity and reliability issues. **Figure 11** depicts the typical placement of C_{IN} and C_{OUT}. It is recommended to keep C_{OUT} to a low value (<<100nF) when possible.

A high C_{OUT} may hinder the ZES100's current sensing, as most of the DUP's dynamic supply current will be drawn from C_{OUT} instead of ZES100. Furthermore, it is strongly recommended that C_{IN} >> C_{OUT} to prevent reverse bias current from V_{OUT} to V_{IN}.

For higher reliability, V_{OUT} should remain lower than V_{IN} such that there is not reversed bias internally.

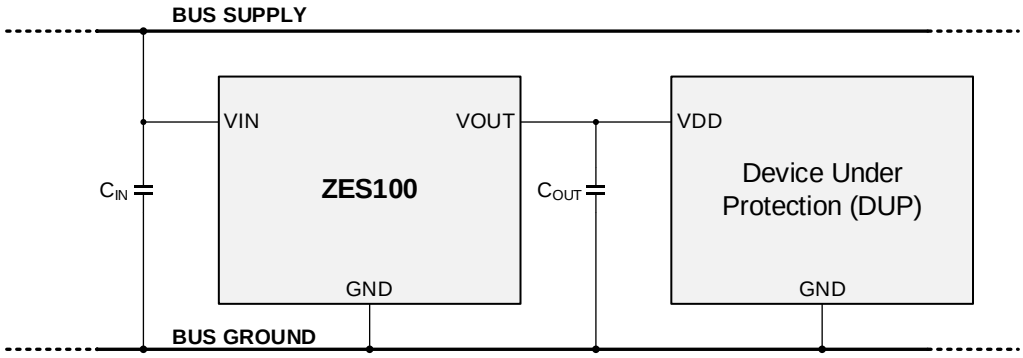


Figure 11 Input and output capacitors placement in a typical application circuit

7 Application Examples

7.1 External Control (MCU/FPGA) of Power Cycling (counting SEL occurrence)

In some applications, there is a need for extra flexibility in controlling the power cycling sequence as it could be disruptive to other parts in a system. There are several ways to configure ZES100 for such application.

Figure 12 depicts an example of ZES100 configuration where the recovery sequence (power cycling) is externally controlled by a microcontroller unit MCU. The DRVN pin serves to provide a flag signal to the MCU. DRVN = "1" means an SEL/overcurrent is detected, while DRVN = "0" means no overcurrent/SEL is detected.

When there is SEL/overcurrent flag signal detected by MCU, the MCU can count the number of SEL and delay the power cycling until the suitable time to activate the power cycle.

The MCU can activate the power cycling through both O1 and O2 (Output1 and 2) pins to ZES100 GP and GN pin. GP and GN pins are the gate pin of the internal power PFET and NFET switches, respectively.

O1 = “0” means turn on internal PFET and O2 = “0” means turn off internal NFET switches to turn ON V_{OUT}.

O1 = “1” means turn off internal PFET and O2 = “1” means turn on internal NFET switches to turn OFF V_{OUT}.

When the pull-down switch is unnecessary, the internal NFET switch can be disabled by connecting GN pin to GND instead.

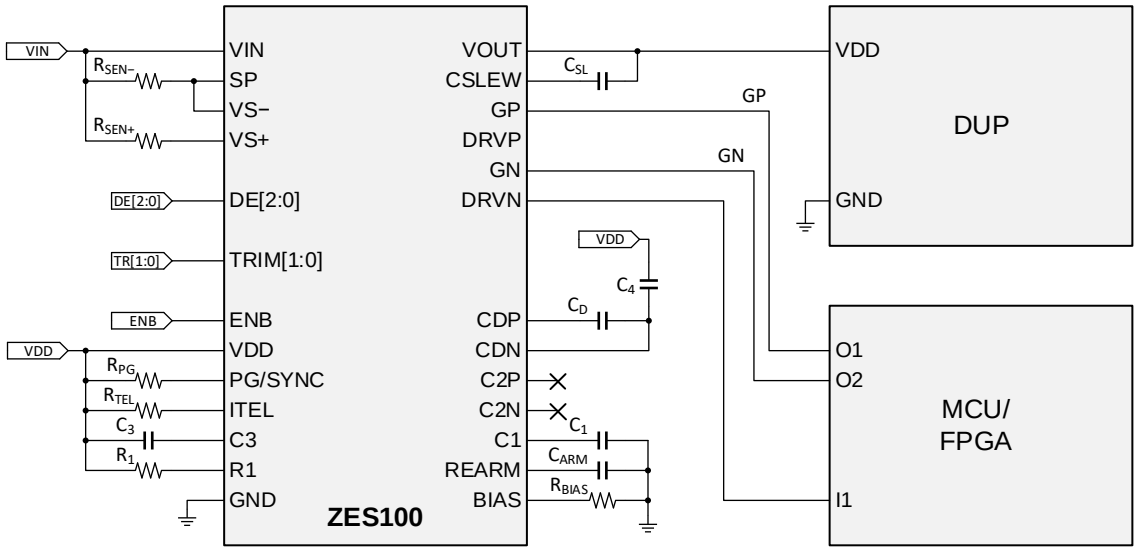


Figure 12 An example of ZES100 configuration with external control of power cycling

7.2 Limit to Single Power Cycle

In some applications, during the over-current state there is a need to just have a single power cycle instead of having power cycling sequence repeated until the overcurrent state is removed.

Figure 13 depicts an example of ZES100 configuration where the recovery sequence (power cycling) is limited to just one single cycle. The PG pin serves to provide a flag signal to the On board computer (OBC). The OBC will disable the ENB pin when there is PG negative pulse detected. This will limit the power cycling sequence from repeated.

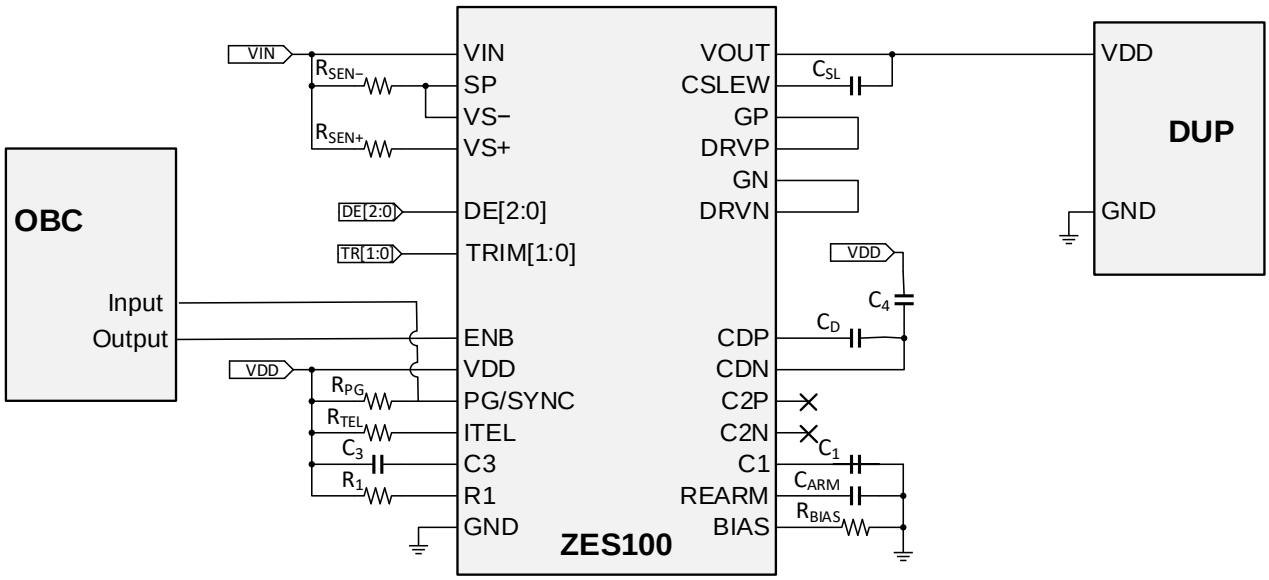
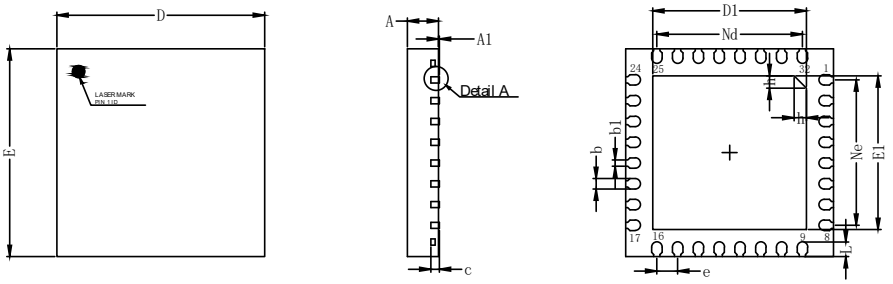
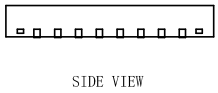


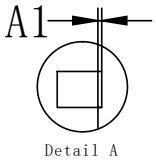
Figure 13 An example of ZES100 configuration with Single power cycle

8 Package Information

8.1 Package Outline (QFN32L 5mm×5mm)

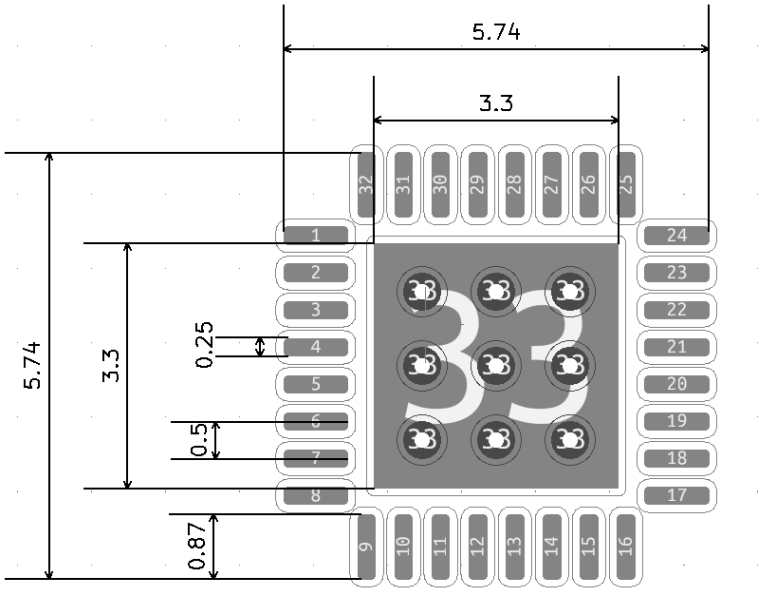






SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.20	0.25	0.30
b1	0.150REF		
c	0.203REF		
D	4.90	5.00	5.10
D1	3.60	3.70	3.80
e	0.50BSC		
Ne	3.50BSC		
Nd	3.50BSC		
E	4.90	5.00	5.10
E1	3.60	3.70	3.80
L	0.30	0.35	0.40
h	0.25	0.30	0.35

8.2 Land Pattern (QFN32L 5mm×5mm)



Dimensions are in millimeters
Recommended dimensions for thermal vias:
pad size: 1mm
hole size: 0.5mm
pitch: 1mm

8.3 Tape and Reel Information (to be updated)

9 Revision History

Version No.	Notes	Date
Rev 0.1	Preliminary version	May, 2022
Rev 1.0	Initial Release	Oct, 2022
Rev 1.1	Added peripheral values	Dec, 2022
Rev 1.2	Recommended schematics amended	June, 2023
Rev 1.3	Removal of Mode selections	Sept, 2023
Rev 1.4	Added current sensing ratio table	Jan, 2024
Rev 1.5	Formula table update	Feb, 2024
Rev 1.6	Ordering part number revision	Apr, 2024
Rev 1.7	ENB = "1", DRVP = V_{DD}, DRVN = V_{DD}. (switch off)	June, 2024
Rev 1.8	Updated with current sensing ratio table	Aug, 2024
Rev 1.9	Added single power cycle application	Oct, 2024

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