Radiation Hardened Quad-Channel Voter ZES400 (QFN28L)

Enabling Advanced Commercial-Off-The-Shelf (COTS) to 'Space-Grade'

1. General Description – Voter ZES400

ZES' Quad-Channel Voter, ZES400, is a radiation hardened monolithic microchip, embodying 4 channels of 3-input majority voters to mitigate the soft errors in digital circuits and systems. It can be applied to support a Triple-Modular-Redundancy (TMR) system.

ZES400 is fabricated in a 130nm CMOS, and is designed based on ZES' proprietary Radiation-Hardened-By-Design (RHBD) technologies, offering high radiation tolerance. It embodies four independent 3-input majority gates where each gate has its own individual error indication output. ZES400 can operate from 1.8V to 5V.

ZES400 is immune to Single-Event-Latchup (SEL), Single-Event Transient (SET), and is unaffected by long-term drift current due to Total Ionized Dose (TID).

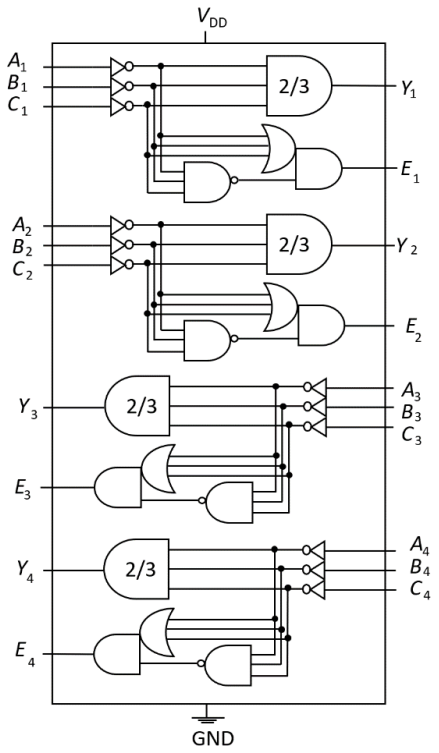
ZES400 is suitable for applications such as space/satellite, medical, etc., that critically require high reliability and high radiation tolerance.

1.1 Features

- ❑ 1.8 to 5 VDC power supply voltage operation
- ❑ Inputs tolerant up to 5.5 VDC at any V_{DD}
- ❑ Provide logic-level down translation to V_{DD}
- ❑ Extended operating temperature range (-55 °C to +125 °C)
- ❑ Package available: QFN28
- ❑ Space qualified technology
- ❑ Radiation-Hardening-by-Design (RHBD)
- ❑ TID tested up to 300 krad (Si) @ Co-60
- ❑ SEL tested up to 110.1 MeV.cm^2/mg @ Heavy-ion
- ❑ SET tested up to 83.3 MeV.cm^2/mg @ Heavy-ion
- ❑ SEL/SET tolerance tested up to 4,600pJ laser energy (@1064nm laser wavelength)
- ❑ ITAR-free
- ❑ Qualified for space enhanced plastic (SEP)
  - MIL-STD-883-2-2019-Method 2030
  - JESD22-A113I-2020
  - JESD22-A104F-2020
  - JESD22-A118B.01-2021
  - JESD74A-2007
  - JESD22-A108G-2022

2. Logic Diagram

The ZES400 logic diagram is depicted as below.



2/3 – indicating a 3-input majority gate

Fig. 1: Qual-Channel Voter Schematic (A_i, B_i & C_i are inputs, Y_i is the majority gate output, E_i is the error indication output - i is the channel number)

3. Logic Data

The ZES400 truth table is tabulated below. '1' indicates the high logic level, and '0' indicates the low logic level. The subscript i refers to the channel number of the voter.

Input			Output	
A_i	B_i	C_i	Y_i	E_i
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	1
1	0	0	0	1
1	0	1	1	1
1	1	0	1	1
1	1	1	1	0

4. Ordering Information

Ordering Information

PART	Grade	Package	Size
ZES400VOTFQ-EP	Space Plastic Flight Model	QFN28L	5mm × 5mm
ZES400VOTGQ-EP	Space Plastic Ground Model*	QFN28L	5mm × 5mm
ZES400VOTGEV-EP	Evaluation Module*	PCB	14cmx12.8cm

* These units are intended for engineering evaluation only. These units are not suitable for qualification, production, radiation testing or flight use. Parts are only tested in room temperature, and hence not warranted for performance over the full specified temperature range of –55°C to 125°C or operating life.

For price, delivery, and ordering information please contact info@zero-errorsystems.com

5. Package Pin Configuration

5.1 QFN28 Package Pin Configuration

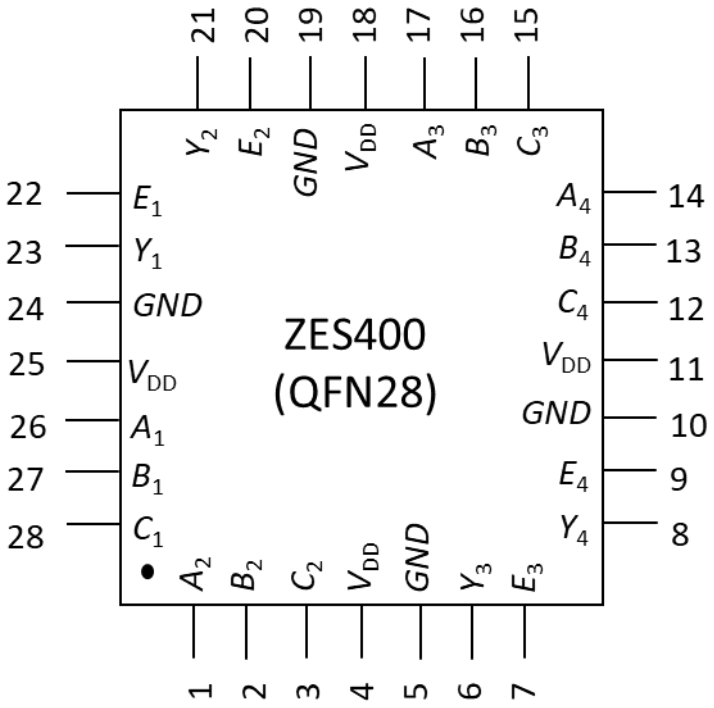


Figure 2: Pin Configuration for QFN28

List of Pins

Pin No.	Name	Type	Description
1	A_2	Input	1st input of the voter channel 2
2	B_2	Input	2nd input of the voter channel 2
3	C_2	Input	3rd input of the voter channel 2
4	V_{DD}	Supply	DC Power Supply
5	GND	Supply	Ground
6	Y_3	Output	Majority gate output of the voter channel 3
7	E_3	Output	Voter error output of the voter channel 3
8	Y_4	Output	Majority gate output of the voter channel 4
9	E_4	Output	Voter error output of the voter channel 4
10	GND	Supply	Ground
11	V_{DD}	Supply	DC Power Supply
12	C_4	Input	3rd input of the voter channel 4
13	B_4	Input	2nd input of the voter channel 4
14	A_4	Input	1st input of the voter channel 4
15	C_3	Input	3rd input of the voter channel 3
16	B_3	Input	2nd input of the voter channel 3
17	A_3	Input	1st input of the voter channel 3
18	V_{DD}	Supply	DC Power Supply
19	GND	Supply	Ground
20	E_2	Output	Voter error output of the voter channel 2
21	Y_2	Output	Majority gate output of the voter channel 2
22	E_1	Output	Voter error output of the voter channel 1
23	Y_1	Output	Majority gate output of the voter channel 1
24	GND	Supply	Ground
25	V_{DD}	Supply	DC Power Supply
26	A_1	Input	1st input of the voter channel 1
27	B_1	Input	2nd input of the voter channel 1
28	C_1	Input	3rd input of the voter channel 1

6. Electrical Characteristics

The sign convention for current follows JEDEC standards with negative values representing current sourced from the device and positive values representing current sunk into the device.

6.1 Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
T_{st}	Store temperature range	-65	+150	°C
T_j	Operating junction temperature range	-55	+150	°C
V_{ESD}	ESD capability, human body model	0	2k	V
V_{DD}	Power supply	-0.5	5.5	V
A_i, B_i, C_i	Digital input	-0.5	5.5	V
Y_i, E_i	Digital output	0	V_{DD}+0.5(1)	V
I_O	Continuous output current (per pin)	0	16	mA
I_{CC}	Maximum supply current	0	130	mA

(1) Digital output Y_i, E_i must remain below absolute maximum rating of V_{DD}

6.2 Recommended operating conditions

Symbol	Parameter		Min	Max	Unit
V_{DD}	Voltage supply of the core		1.8	5.0	V
V_I	Input voltage		0	V_{DD}	V
V_O	Output voltage		0	V_{DD}	V
V_{IH}	High-level input voltage	V_{DD}=1.8±10% V	1.2	-	V
		V_{DD}=5.0±10% V	3.5	-	V
V_{IL}	Low-level input voltage	V_{DD}=1.8±10% V	-	0.7	V
		V_{DD}=5.0±10% V	-	1.5	V
I_{OH}	High-level output current	V_{DD}=1.8±10% V	-	-2	mA
		V_{DD}=5.0±10% V	-	-4	mA
I_{OL}	Low-level output current	V_{DD}=1.8±10% V	-	2	mA
		V_{DD}=5.0±10% V	-	4	mA
t_r, t_f	Input rise or fall time (10% to 90%)	V_{DD}=1.8±10% V	-	1000	ns
		V_{DD}=5.0±10% V	-	400	ns

6.3 Thermal Information

Symbol	Parameter	Min	Typ.	Max	Units
T_J	Operating junction temperature	-55	-	+125	°C
$R_{\theta JA}$	Junction to ambient thermal resistance for QFN28L(5x5x0.75 , t0.5) package	-	47	-	°C/W

6.4 Static Characteristics

DC Electrical Characteristics

Symbol	Parameter	Test Conditions	V_{DD}	Min	Typ.	Max	Unit
V_{OL}	Low-level output voltage	I_O = 100 µA	1.65 to 5.5	0.025	0.032	0.04	V
		I_O = 1 mA	1.65 to 5.5	0.29	0.32	0.35	V
		I_O = 2 mA	1.65 V	-	0.55	0.58	V
			3.0 V	-	0.54	0.57	V
			4.5 V	-	0.54	0.57	V
		I_O = 4 mA	3.0 V	-	0.92	0.95	V
			4.5 V	-	0.96	0.99	V
V_{OH}	High-level output voltage	I_O = -100 µA	1.65 to 5.5	V_{DD}-0.06	V_{DD}-0.04	V_{DD}-0.03	V
		I_O = -1 mA	1.65 to 5.5	V_{DD}-0.37	V_{DD}-0.33	V_{DD}-0.29	V
		I_O = -2 mA	1.65 V	1.02	1.05	-	V
			3.0 V	2.40	2.43	-	V
			4.5 V	3.90	3.94	-	V
		I_O = -4 mA	3.0 V	2.00	2.03	-	V
			4.5 V	3.45	3.48	-	V
I_{CC}	Quiescent supply current	*VI = GND* *IO = 0 mA*	5.5 V	0.5	0.7	1.6	µA

6.5 Dynamic Characteristics

AC Electrical Characteristics

Symbol	Parameter	Conditions	V_{DD}	Min	Typ	Max	Unit
t_{pd_Y}	Propagation Delay for output *Y*	25°C, 50pF Load	5.0 V	20	23	26	ns
			3.3 V	24	27	30	ns
			1.8 V	38	42	46	ns
t_{pd_E}	Propagation Delay for output *E*	25°C, 50pF Load	5.0 V	19	22	25	ns
			3.3 V	22	26	31	ns
			1.8 V	35	39	44	ns
C_{in}	Input Capacitance	V_I = V_{DD} or *GND*	1.65 to 5.5 V	-	-	-	pF
C_{pd}	Power dissipation capacitance	I_O = 0 mA f = 1 MHz *1 Channel Core	5V	9	10	11	pF

6.6 Radiation Test Results

The radiation hardness results are summarized below. For detailed radiation test results, please contact info@zero-errorsystems.com

Parameter	Condition	Value*	Units
Total Ionizing Dose (TID)	Co-60 @ V_{DD}=5V, room temp (TID facility @ Kyushu University ITO)	Up to 300	krad (Si)
SEL Linear Energy Transfer (LET)	Heavy-Ion @ V_{DD}=5V, 125°C (Cyclotron @ Texas A&M University)	Up to 110.1	MeV-cm^2/mg
SET LET	Heavy-Ion @ V_{DD}=1.8V, room temp (Cyclotron @ Texas A&M University)	Up to 83.3	MeV-cm^2/mg
SEL Laser energy	Laser wavelength 1064nm @ V_{DD} =5V	Up to 4,600	pJ
SET Laser energy	Laser wavelength 1064nm @ V_{DD} =1.8V	Up to 4,600	pJ

* The value was the characterized value during the test, and no abnormal changes (e.g., TID, SEL, SET) were observed.

6.7 Characteristics Measurement Information

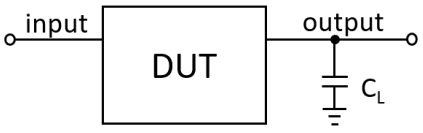


Figure 3: Load Circuit

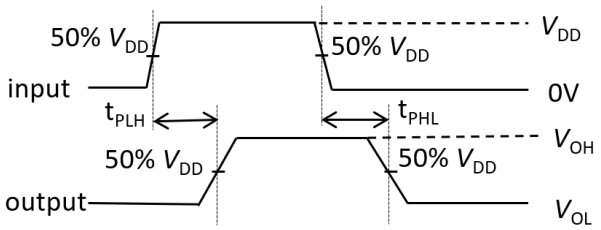


Figure 4: Propagation Delay Measurement

7 Device Description and Operation

ZES400 is a quad-channel three-input majority gate, having four independent three-input majority gate and their corresponding error indication otuputs. It can be used in a Triple-Modular-Reduncancy (TMR) system. For each channel, if 2 out of 3 inputs are the same logic level, the majority gate will generate the ouput having the same logic level. Its corresponding error indication will generate the high logic level if at least one of the 3 inputs is diffferent in the logic level. It is recommended to operate with a supply voltage ranging from 1.8V to 5V.

8 Application Information

ZES400 is intended to allow a Triple-Modular-Reduncancy (TMR) implementation to exchange data between two sub-systems, aiming to achieve an error-free data transfer. Fig. 5 depicts an example how the data can be exchanged, via ZES400, between the two sub-systems A and B. In the sub-system A, three sub-circuits T1, T2 and T3 generate three same signals T_a, T_b, and T_c which are voted by ZES400 to generate a voted ouput T_y. The three sub-circuits T1, T2 and T3 are usually the same. The voted output T_y is virtually glitch-free bacause the ZES400 is virtually SET-free. The voter output T_y is virtually error-free provided that the error possibility to have two errornos signals (out of the three signals T_a, T_b, and T_c) is assumed to be very low. The error indication signal T_e can be used to allert the sub-system B, indicating that at least one of the three signals T_a, T_b, and T_c is different.

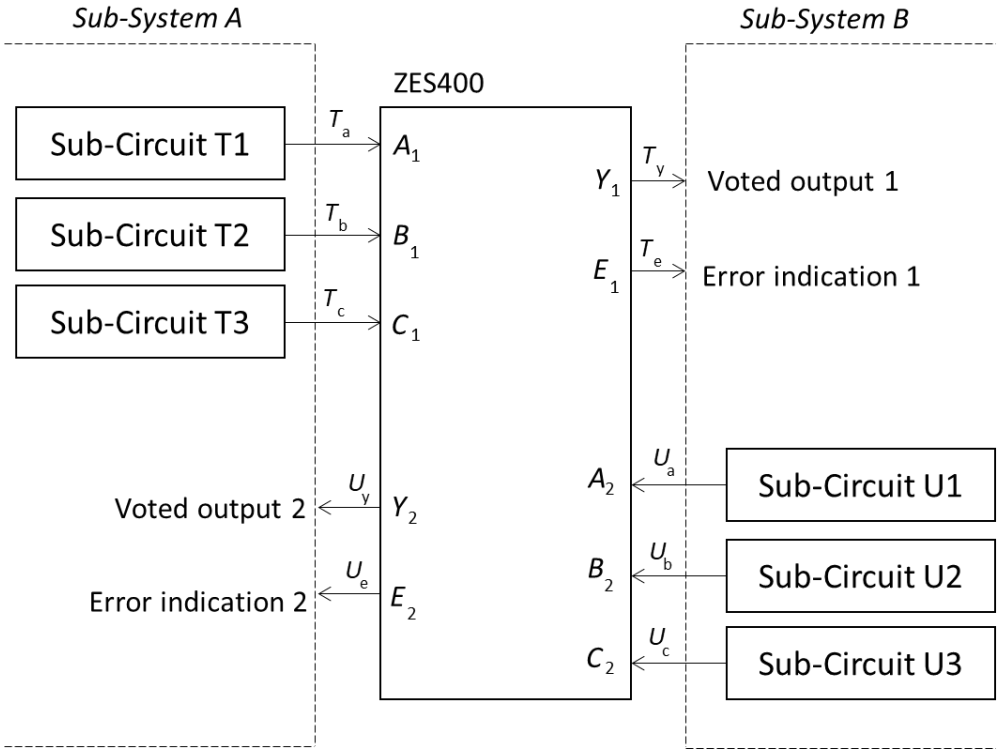


Figure 5: ZES400 aplication example

Similarly, in the sub-system B, three sub-circuits U1, U2 and U3 generate three same signals U_a, U_b, and U_c which are voted by ZES400 to generate a voted ouput U_y. The three sub-circuits U1, U2 and U3 are usually the same. The voted output U_y is virtually glitch-free bacause the ZES400 is virtually SET-free. The voter output U_y is virtually error-free provided that the error possibility to have two errornos signals (out of the three signals U_a, U_b, and U_c) is assumed to be very low. The error indication signal U_e can be used to allert the sub-system A, indicating that at least one of the three signals U_a, U_b, and U_c is different.

8.1 Application Examples

ZES400 can be applied to a critical data bus with various communcation protocols. Some communication protocol examples include UART, SPI, etc.

For the detailed implementations for these communication protocols with ZES400, please contact info@zero-errorsystems.com.

Hardware/software co-solution for enabling ZES Error Detection-and-Correction (ZEDAC) algorithm

ZES400 with FRAM (3pcs) can be integrated with the ZES error-detection-and-correction (ZEDAC) algorithm(s) to enable data protection virtually for any memories (e.g., eMMC or DRR4). Fig. 6 briefly depicts the interface setup where a processing unit embodying either a microcontroller (MCU) or an FPGA. The processing unit is interfaced with an external memory and ZES400 with FRAMS (3pcs). The external memory could be a Commercially-Off-the-Shelf (COTS) memory (e.g.., eMMC or DDR4) whose data need to be protected. The ZEDAC algorithm is executed within the MCU/FPGA, providing the encoding/decoding process. The ZES400 and the ZEDAC algorithm collectively serve as a hardware/software co-solution to reduce the soft-error (e.g., bit flips) in the external memory. The hardware/software co-solution provides 50x better error-rate than the hardware-only solution, and 2000x better error-rate than the solution-only solution. For more information about ZEDAC, please contact info@zero-errorsystems.com

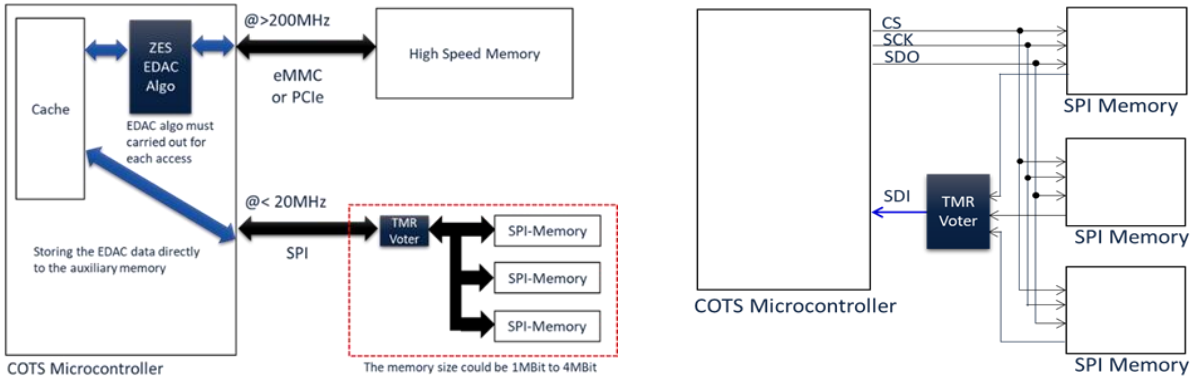


Fig. 6 Triple-modular-redundancy(TMR) application via Voter-IC (ZES400)

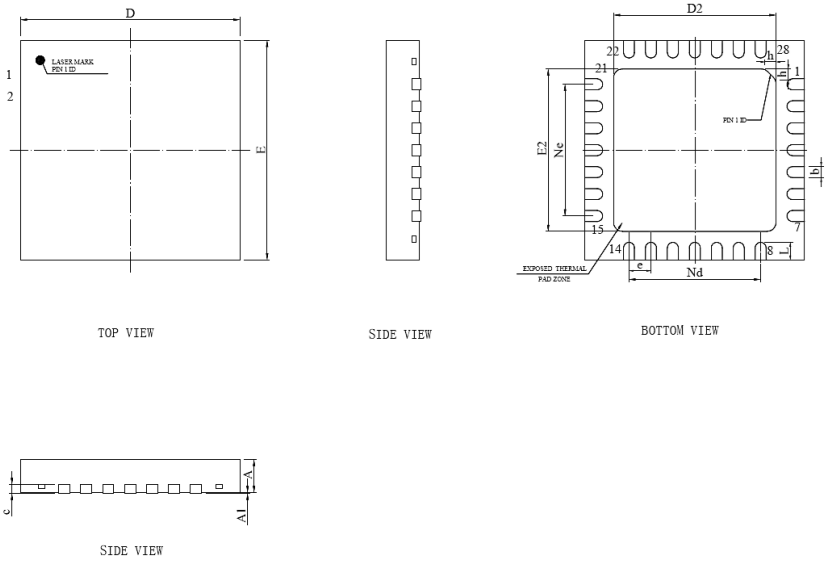
8.2 Application Tips

All unused **inputs** must **not** be left floating. They may be connected to either a low (*GND*) or high (V_{DD}) bias to provide a known state at the input of the device. Resistors may be used to tie off unused inputs.

An unused **output** may be left floating. It is suggested that it be routed to a test point or similar accessible point.

9 Package Information

QFN28L (5x5x0.75-0.5)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	--	0.02	0.05
b	0.20	0.25	0.30
c		0.203REF	
D	4.90	5.00	5.10
D2	3.60	3.70	3.80
e		0.50BSC	
Ne		3.00BSC	
Nd		3.00BSC	
E	4.90	5.00	5.10
E2	3.60	3.70	3.80
L	0.35	0.40	0.45
h	0.25	0.30	0.35

Figure 7: Dimension of QFN28L (5mmx5mmx0.75mm-0.5)

10 Reliability Test

ZES400 space plastic flight model (ZES400VOTFQ-EP) is tested for the space enhanced plastic (SEP) specifications. The following tests were conducted.

Scanning Acoustic Tomography (SAT): Test Method MIL-STD-883-2-2019-Method 2030
Preconditioning: Test Method JESD22-A113I-2020 (Temperature Cycle, Bake, Soak, Reflow)
Temperature Cycle (TC): Test Method JESD22-A104F-2020
UHAST: Test Method JESD22-A118B.01-2021
ELRF: Test Method JESD74A-2007
HTOL: Test Method JESD22-A108G-2022
Three-Temperature Test: -55°C, 25°C & 125°C (for all functional tests, and after TC, UHAST, ELRF, & HTOL)

ZES400 space plastic ground model (ZES400VOTGQ-EP) is only tested for functional testing at room temperature.

11 Revision History

Version	Description	Date
V1.0	Preliminary version	Jan-2022
V1.1	P10 and P24 amended to Ground, P11 and P25 amended to VDD.	Feb-2022
V1.2	Company logo and disclaimer updated.	Apr-2022
V1.3	Package information updated to QFN28L (5x5x0.75-0.5).	Aug-2022
V1.4	Heavy-Ion SEE test results included. Laser SEE test results included. Electrical test results updated	Sep-2022
V1.5	TID test results included Characterized test results updated Reliability test information included Logic diagram updated	June-2023
V1.6	Ground model part number updated	Aug-2023
V1.7	Fig. 2 is updated with a new orientation Flight and ground models are updated with reliability test conditions Ordering information for the evaluation module is included	Jan-2024
V1.8	Part numbers are updated	Feb-2024
V1.9a	Power dissipation capacitance is updated	Oct-2024

For the latest version of this document, please contact us info@zero-errorsystems.com.

12 Legal

All products, product specificatios and data are subject to change without notice.

IMPORTANT NOTICE AND DISCLAIMER

ZES PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with ZES products. You are solely responsible for (1) selecting the appropriate ZES products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. ZES grants you permission to use these resources only for development of an application that uses the ZES products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other ZES intellectual property right or to any third-party intellectual property right. ZES disclaims responsibility for, and you will fully indemnify ZES and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

ZES’ products are provided subject to ZES’ Terms of Sale or other applicable terms available either on zero-errorsystems.com or provided in conjunction with such ZES products. ZES’ provision of these resources does not expand or otherwise alter ZES’ applicable warranties or warranty disclaimers for ZES products. ZES objects to and rejects any additional or different terms you may have proposed.