# ZES302 - Radiation Hardened Point-of-Load (PoL)

**Enabling Advanced Commercial-Off-The-Shelf (COTS) to 'Space-Grade'**

## Description

ZES302, Point-of-Load (PoL) is a radiation-hardened high efficiency synchronous buck regulator with integrated power transistors that can deliver up to 3A of output current. This single chip operates over an input voltage of 3V to 5.5V and provides a regulated output voltage that is externally adjustable from 0.8V to $PV_{IN}$−0.8V.

ZES's PoL based on proprietary technology (patent pending) offers an unprecedented means to supply power to COTS. Specifically, ZES's PoL embodies a unique control mode, hence featuring optimized power efficiency over a wide loading range, zero current switching, ultra-fast transient response, and over current protection. Further, multiple of ZES's PoLs can be placed in parallel, hence exhibiting innate redundancy.

PoL is realized with Radiation Hardening By Design (RHBD) approach, hence highly tolerant to various radiation effects in space.

High integration makes PoL an ideal candidate to supply DC power to advanced ICs in space.

## Applications

- Battery Operated Equipment
- Regulated Voltage Source
- Board Level Local Power Conversion
- Embedded systems

## Features

- Integrated power transistors
- 3A maximum output current
- Optimized high power efficiency, >92% peak
- 'Plug-and-play' parallel operation with redundancy
- Configurable Soft-Start
- Innate over-current protection
- Power-good output voltage monitor
- Compatible with small size inductor Fast transient
- Full Mil-temp range operation ($T_A$ = −55°C to +125°C)
- Qualified for Space Enhanced Plastic (SEP)
- Space qualified technology
- Radiation Hardened by Design (RHBD)
- ITAR free

### Electrical Performance

| | |
|---|---|
| Input Voltage | 3V to 5.5V |
| Output Voltage | 0.8V to $PV_{IN}$−0.8V |
| Maximum Output Current | 3A |
| Switching Frequency | ≤2MHz |
| Peak Power Efficiency | >92% |
| Output Ripple (CCM) | <10mVpp |

### Radiation Performance (Cyclotron Verified)

| | |
|---|---|
| TID | 100 Krad (Si) |
| SEL | 90 MeV-cm$^2$/mg |
| SEFI | 60 MeV-cm$^2$/mg |
| SEU | 60 MeV-cm$^2$/mg |
| Ion Fluence | Up to $10^7$/cm$^2$ |

### Ordering Information

| Part No. | Grade | Form Factor | Size |
|---|---|---|---|
| ZES302POLFQ-EP | Space Plastic Flight Model | QFN40L | 5 mm × 5 mm |
| ZES302POLGQ-EP | Ground Model* | QFN40L | 5 mm × 5 mm |
| ZES302POLGEV-EP | Space Plastic Evaluation Board* | PCB | 100 mm x 100mm |

**For price, delivery, and ordering information please contact info@zero-errorsystems.com.**

* These units are intended for engineering evaluation only. These units are not suitable for qualification, production, radiation testing or flight use. Parts are not warranted for performance over the full specified temperature range of –55°C to 125°C or operating life.

## Typical Application

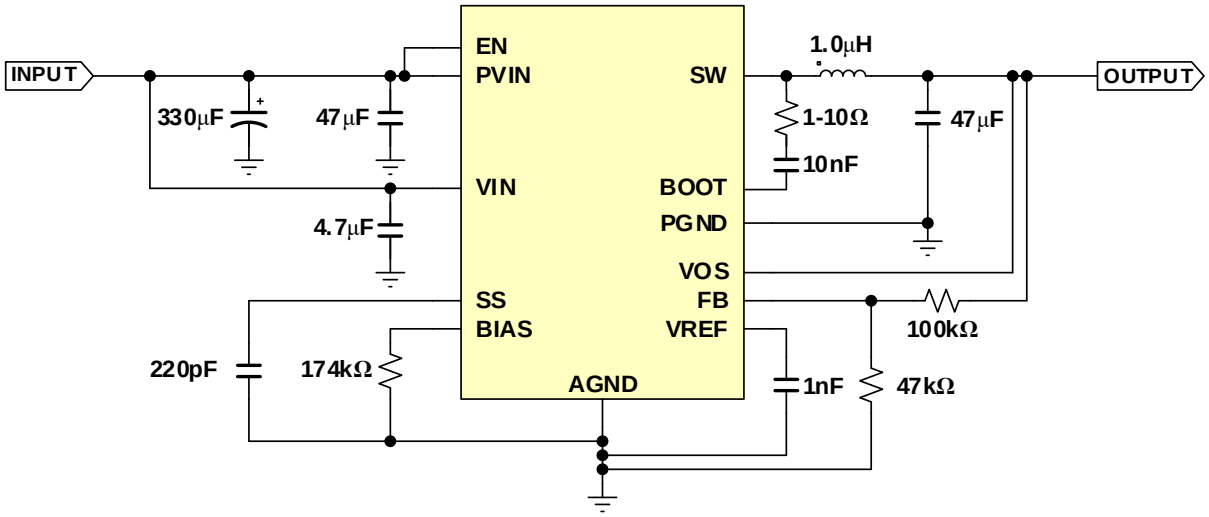
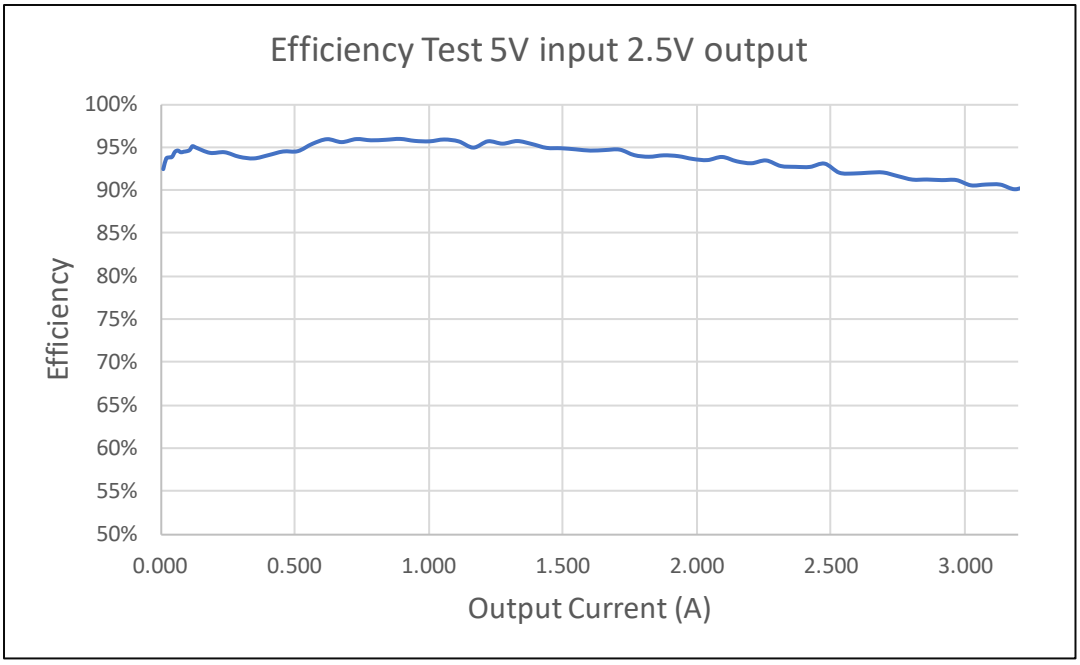
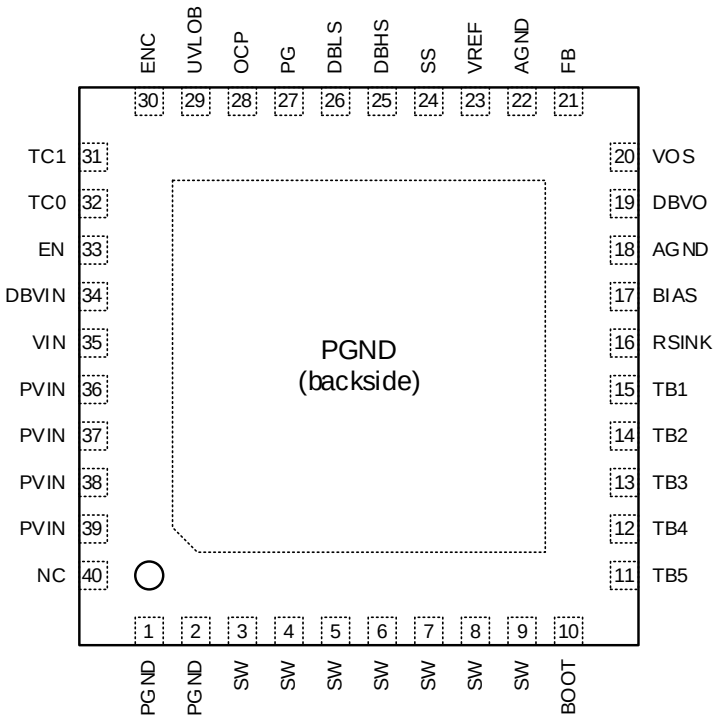



**Figure 1 Simplified typical application schematic for $V_{OUT}$ of 2.5V**

## Efficiency



## 2.1 Pin Configuration




## 2.2 Pin Description Table

| Pin | Name | Type | Description |
|---|---|---|---|
| 1-2, EP | PGND | Ground | Power Ground Pin |
| 3-9 | SW | Output | Switching Node Output pin |
| 10 | BOOT | Power | Bootstrap Capacitor pin |
| 11-15 | TB5..TB1* (MSB..LSB) | Analog I/O | VREF Trimming pins |
| 16 | RSINK* | Analog I/O | Sink Resistor pin |
| 17 | BIAS* | Analog I/O | Bias Resistor pin |
| 18, 22 | AGND | GND | Analog Common Ground pin |
| 20 | VOS | Input | VOUT sense |
| 21 | FB | Input | Feedback Input pin |
| 23 | VREF | Output | Reference Voltage Output pin |
| 24 | SS | Analog I/O | Soft Start pin |
| 27 | PG | Output | Power Good pin |
| 28 | OCP* | Debug | Over Current Protect Debug pin |
| 29 | UVLOB* | Debug | Under Voltage Lockout Debug pin |
| 31-32 | TC1..TC2* | Analog I/O | Current Sensing Trimming pin |
| 33 | EN | Input | Enable Input pin |
| 35 | VIN | Power | Analog Supply Voltage pin. |
| 36-39 | PVIN | Power | Power Supply |
| 19,25,26,30,34,40 | NC | Analog Out | Analog Output Debug Pin |

* These pins will be removed in the future.

## 3.1 Functional Block Diagram

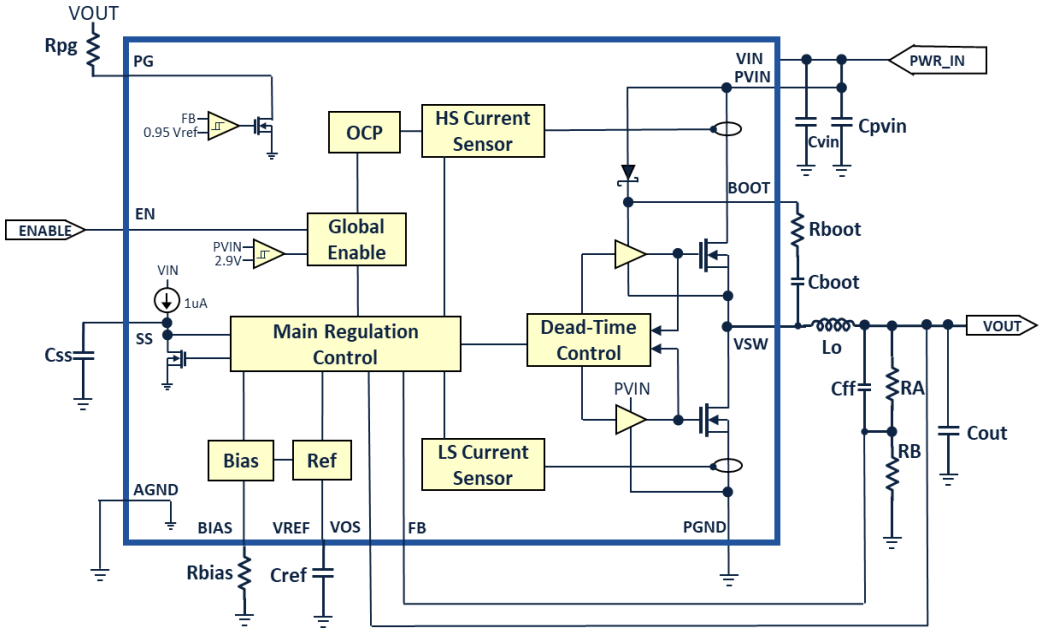



**Figure 2 Functional block diagram.**

PRELIMINARY

## 3.2 Integrated Circuit Operation:

ZES302 is a synchronous DCDC buck regulator integrated circuit. The control system embodies both a voltage-mode hysteretic control (VMHC) and current-mode hysteretic control (CMHC). The first advantage of this design is that the buck converter can operate in both DCM and CCM and thus provide excellent efficiency at both light and heavy loads. The second advantage is that unlike traditional current-mode PWM controller, the linear regulation in our design only works when the buck converter enters heavy load. Thus, the error amplifier compensation network in CMHC can be easily designed since the output pole at heavy load is at much higher frequency and can be cancelled easily with an on-chip zero, leading to a system that is close to a single pole system with much higher bandwidth. This also gives rise to fast transient responses. Besides, the proposed design achieves a quasi-fixed switching frequency to ensure predictable EMI performance without any clock generator.

## 3.3 Pin Functions

**AGND: Analog GND pin(s).** Internal analog circuit blocks ground pin and the IC output voltage negative terminal for the Cout and RB output sensing resistor.

**BIAS: Bias reference Pin**. A resistor is connected here to ground to provide the internal analog block reference current of 500nA. A 174k ohm resistor is the recommended value. Pin will be removed in the future versions of this IC.

**VREF: Voltage Reference Pin** is the internal comparator input pin. The voltage of 0.8V is set internally. a 100nF capacitor is recommended for Cref.

**FB: Feedback Pin** Connect a resistor from FB to VOUT and FB to GND to adjust the output voltage in accordance with the following equation.

$$V_{OUT} = V_{REF}\left(1 + \frac{R_A}{R_B}\right)$$

$V_{OUT}$ = Output voltage,
$V_{REF}$ = Reference voltage (0.8V typical)
$R_A$ = Top divider resistor, and
$R_B$ = Bottom divider resistor.

**VOS: VOut sense Pin,** an internal divider is connected to this pin for the Main Regulation Control circuit to measure the Vout voltage.

**PGND: Power Ground Pin** is the return path of the internal power transistor synchronous switch. Please provide a large continuous PCB area for this pin and connect the Cout capacitor terminal and CPVIN Capacitor nearest to this pin(s).

**VSW: Switching Voltage Output Pin:** The switching internal power transistors output pin. Connect this pin(s) to the inductor with a wide trace.

**BOOT: Bootstrap Pin:** A series resistor and capacitor is connected to this pin and VSW. This pin provides the required drive voltage for the power transistor switch. A capacitor of 10nF to 100nF and a series resistor of 1 Ohm to 10 ohms are recommended.

**PVIN: Power Voltage Input pin.** This pin is the input terminal for the internal high side transistor switch. Please provide a large area for this pin and connect the CVIN Capacitor to this pin.

**VIN: Analog Voltage input pin.** Most of the Analog circuitry is connected to this pin. A decoupling capacitor (CVIN) of 4.7uF is recommended to be connected to this pin and ground.

**PG: Power Good Pin**. This pin has an open drain Mosfet transistor. The pin will remain low until 0.95 VREF is detected at the FB pin. A 100K resistor is recommended for the pull up resistor (Rpg).

**EN: ENABLE Pin.** This pin enables the operation of the regulator typically this pin is connected to VIN. The threshold can be adjusted by a resistor divider connected to VIN and GND. Typical enable voltage is 0.8V lower than 0.6V the DCDC is in shutdown mode.

**SS: SOFT START Pin.** This pin enables the soft start operation of the regulator. A 220pF capacitor (Css) is typically used.

**PRELIMINARY**

## 3.1 Maximum Ratings

Absolute maximum ratings are limits beyond which damage to the device may occur. Exposure to absolute rating conditions for extended periods may affect device reliability. Functional operation of the device at these conditions is not implied.

**Table 1 Absolute maximum ratings**

| Parameter | Min | Max | Unit |
|---|---|---|---|
| PVIN | − 0.3 | + 5.5 | V |
| SW | − 0.3 | + 5.5 | V |
| PG | − 0.3 | + 5.5 | V |
| VIN | − 0.3 | + 5.5 | V |
| Signal pins† | − 0.3 | + 0.3 | V |
| Storage temperature $T_{STG}$ | −55 | +150 | ℃ |
| Operating Junction Temperature $T_J$ | | | ℃ |
| Thermal resistance junction-case | | | ℃/W |

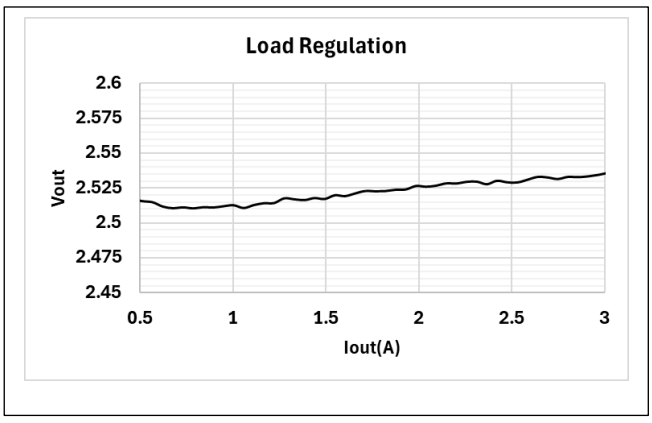
## 3.1 ESD Ratings

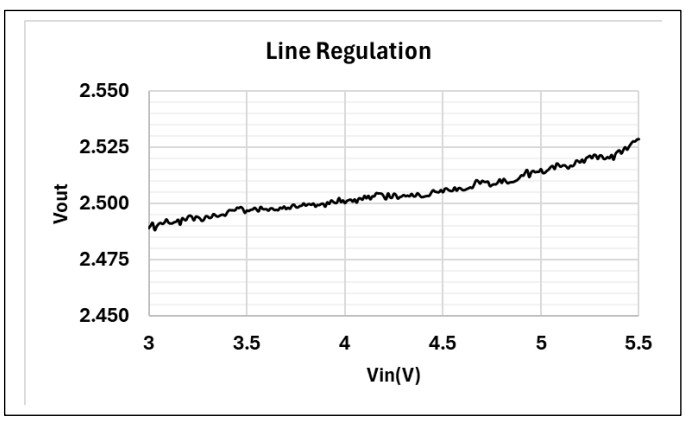
| Parameter | Test Conditions | Value | Unit |
|---|---|---|---|
| ESD Susceptibility | Human Body Model | ± 2000 | V |
| | Charge Device Model | ± 1000 | V |
| | Machine Model | ± 200 | V |

# 4 Electrical Characteristics

Typical values correspond to $T_J$ = 25C. $PV_{IN}$ = $V_{IN}$ = 5V, $V_{OUT}$ = 2.5V, $L_O$ = 1.0µH, $C_O$ = 47µF unless otherwise specified.

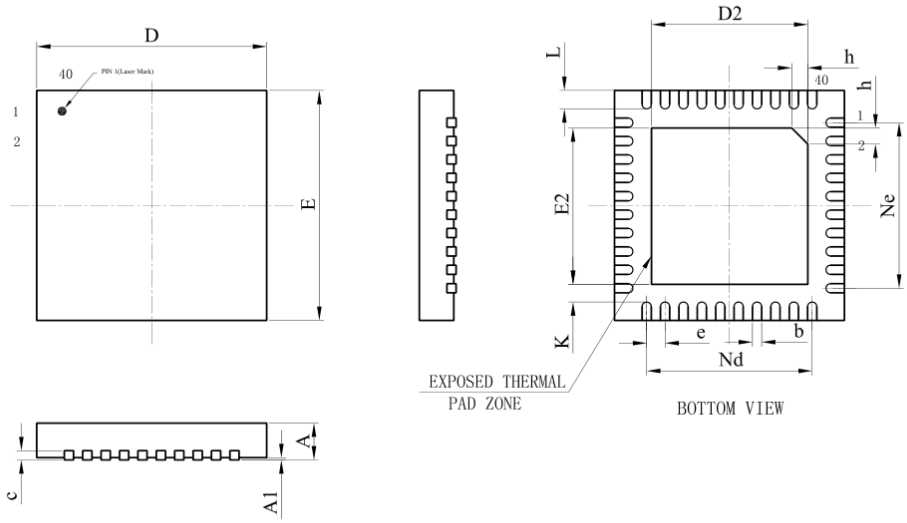
| | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | **Supply Specifications** | | | | | |
| 1 | Input Voltage $PV_{IN}$ | | 3.0 | 5.0 | 5.5 | V |
| 2 | Supply Voltage $V_{IN}$ | | | $PV_{IN}$ | | V |
| 3 | Quiescent Current $I_Q$ | | | 55 | | µA |
| 4 | Shutdown Current | | | 40 | | µA |
| 5 | Enable Pin Voltage | | 0.8 | | Vin | V |
| 6 | **Under Voltage Lockout** | | | | | |
| | Rising Threshold | | | 2.9 | | V |
| | Falling Threshold | | | 2.7 | | V |
| | **Output Specifications** | | | | | |
| 7 | Output Voltage $V_{OUT}$ | | 0.8 | | $V_{IN}$ – 0.8 | V |
| 8 | Output Current $I_{OUT}$ | | | | 3 | A |
| 9 | Load Regulation | | | | 2 | %Vout |
| 10 | Line Regulation | | | | 2 | %Vout |
| 11 | Reference Voltage | | | 0.8 | | V |
| 12 | Output Ripple Voltage | $V_{IN}$ = 5V, $V_{OUT}$ = 2.5V, $I_{OUT}$ = 1mA | | 24 | | mVpp |
| | | $V_{IN}$ = 5V, $V_{OUT}$ = 2.5V, $I_{OUT}$ = 0.1A | | 6 | | mVpp |
| | | $V_{IN}$ = 5V, $V_{OUT}$ = 2.5V, $I_{OUT}$ = 1A | | 6 | | mVpp |
| 13 | High-side FET $R_{DSON}$ | | | 130 | | mΩ |
| 14 | Low-side FET $R_{DSON}$ | | | 70 | | mΩ |
| | **Power Good Signal** | | | | | |
| 15 | Falling Threshold | FB as a % of $V_{REF}$ | | 95 | | % |
| 18 | Output Efficiency | $V_{IN}$ = 5V, $V_{OUT}$ = 2.5V, $I_{OUT}$ = 1mA | | 70 | | % |
| | | $V_{IN}$ = 5V, $V_{OUT}$ = 2.5V, $I_{OUT}$ = 0.1A | | 92 | | % |
| | | $V_{IN}$ = 5V, $V_{OUT}$ = 2.5V, $I_{OUT}$ = 1A | | 93 | | % |
| | | | | | | |



# 5 Package Information

## Package Outline




| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0.70 | 0.75 | 0.80 |
| A1 | — | 0.02 | 0.05 |
| b | 0.15 | 0.20 | 0.25 |
| c | 0.18 | 0.20 | 0.25 |
| D | 4.90 | 5.00 | 5.10 |
| D2 | 3.30 | 3.40 | 3.50 |
| e | 0.40BSC | | |
| Nd | 3.60BSC | | |
| E | 4.90 | 5.00 | 5.10 |
| E2 | 3.30 | 3.40 | 3.50 |
| Ne | 3.60BSC | | |
| L | 0.35 | 0.40 | 0.45 |
| K | 0.20 | — | — |
| h | 0.30 | 0.35 | 0.40 |
| L/F载体尺寸 (mil) | 150*150 | | |

**PRELIMINARY**

## Tape and Reel Information

# 6 Revision History

| Version No. | Notes | Date |
|---|---|---|
| V0.0.65 | Preliminary version | Mar. 2024 |
| V0.0.7 | Ordering information updates | Apr. 2024 |

## Document Changes

1. Update Application
2. Update Specification
3. Explanation of external parts

## IMPORTANT NOTICE AND DISCLAIMER